Rockwell

R6500/41 AND R6500/42 ONE-CHIP INTELLIGENT PERIPHERAL CONTROLLERS

SECTION 1 INTRODUCTION

1.1 FEATURES

- Directly compatible with 6500, 6800, 8080, and Z80 bus families
- Asynchronous Host interface that allows independent clock operation
- Input, Output and Status Registers for CPU/Host data transfer
- Status register for CPU/Host data transfer operations
- Interrupt or polled data interchange with Host
- Enhanced 6502 CPU
  - —Four new bit manipulation instructions:
    - Set Memory Bit (SMB)
    - Reset Memory Bit (RMB)
    - Branch on Bit Set (BBS)
    - Branch on Bit Reset (BBR)
  - —Decimal and binary arithmetic modes
  - —13 addressing modes
  - —True indexing
- 1536-byte mask-programmable ROM
- 64-byte static RAM
- 23 TTL-compatible I/O lines (R6500/41 only)
- 47 TTL-compatible I/O lines (R6500/42 only)
- A 16-bit programmable counter/timer, with latch
  - —Pulse width measurement
  - —Pulse generation
  - —Interval timer
  - —Event counter
- Seven interrupts
  - —Two edge-sensitive lines; one positive, one negative
  - —Reset
  - —Counter Underflow
  - —Host data received
  - —Output Data Register full
  - —Input Data Register empty
- Multiplexed bus expandable to 4K bytes of external memory
- Unmultiplexed bus for Peripheral I/O expansion
- 68% of the instructions are executed in less than 2μs @ 2 MHz
- NMOS-3 silicon gate, depletion load technology
- Single +5V power supply
- 40-pin DIP (R6500/41 only)
- 64-pin QUIP (R6500/42 only)

NOTE

This document describes both the R6500/41 and R6500/42. In the text, the terms IPC or device will be used when describing both parts. The few differences will be described in the text using the terms R6500/41 or R6500/42.

1.2 SUMMARY

The Rockwell R6500/41 and R6500/42 One-Chip Intelligent Peripheral Controllers (IPC) are general purpose, programmable interface I/O devices designed for use with a variety of 8-bit and 16-bit microprocessor systems. The one-chip R6500/41 IPC has an enhanced R6502 CPU, 1.5K by 8-bit ROM, 64 by 8-bit RAM, three I/O ports with multiplexed special functions, and a multi-function timer all contained within a 40-pin package.

For systems requiring additional I/O ports, the device is also available in a 64-pin QUIP version, R6500/42, that provides three additional 8-bit ports. In both versions, special interface registers allow these IPC devices to function as peripheral controllers for the 6500, 6800, Z80, 8080, and other 8-bit or 16-bit host microcomputer systems.

The innovative architecture and the demonstrated high performance of the R6502 CPU, as well as instruction simplicity, results in system cost-effectiveness and a wide range of computational power. These features make the device a leading candidate for IPC computer applications.

To facilitate system and program development for the device Rockwell has developed the R6541Q which can be used as an Emulator. A description of the R6541Q is contained in the R6541Q Product Description (Document Order No. 2136).

Rockwell supports development of the R6500/41 and R6500/42 with the System 65 Microcomputer Development System and the R6500/ ★ Family of Personality Modules. Complete in-circuit emulation with the R6500/ ★ Family of Personality Modules allows total system test and evaluation.

This product description is for the reader familiar with the R6502 CPU hardware and programming capabilities. A detailed description of the R6502 CPU hardware is included in the R6500 Microcomputer System Hardware Manual (Order Number 201). A description of the instruction capabilities of the R6502 CPU is contained in the R6500 Microcomputer System Programming Manual (Order Number 202).

1.3 MASK OPTIONS

The R6500/41 has provision for internal pull-up resistors on PA and PC ports as a mask option. This option is available for port groups only, not for individual port lines.

The R6500/42 has provision for pull-up resistors on PA, PC, PF, and PG ports as a mask option. This option is available for port groups only, not for individual port lines.

SECTION 2
INTERFACE REQUIREMENTS

This section describes the interface requirements for the Intelligent Peripheral Controller. Figure 2-1 is the Interface Diagram for the devices. Figures 2-2 and 2-4 show the pin out configurations and Table 2-1 describes the function of each pin of the devices. Figures 2-3 and 2-5 show the mechanical dimensions of the devices. Section 5 describes the Host computer interface protocol and timing requirements.

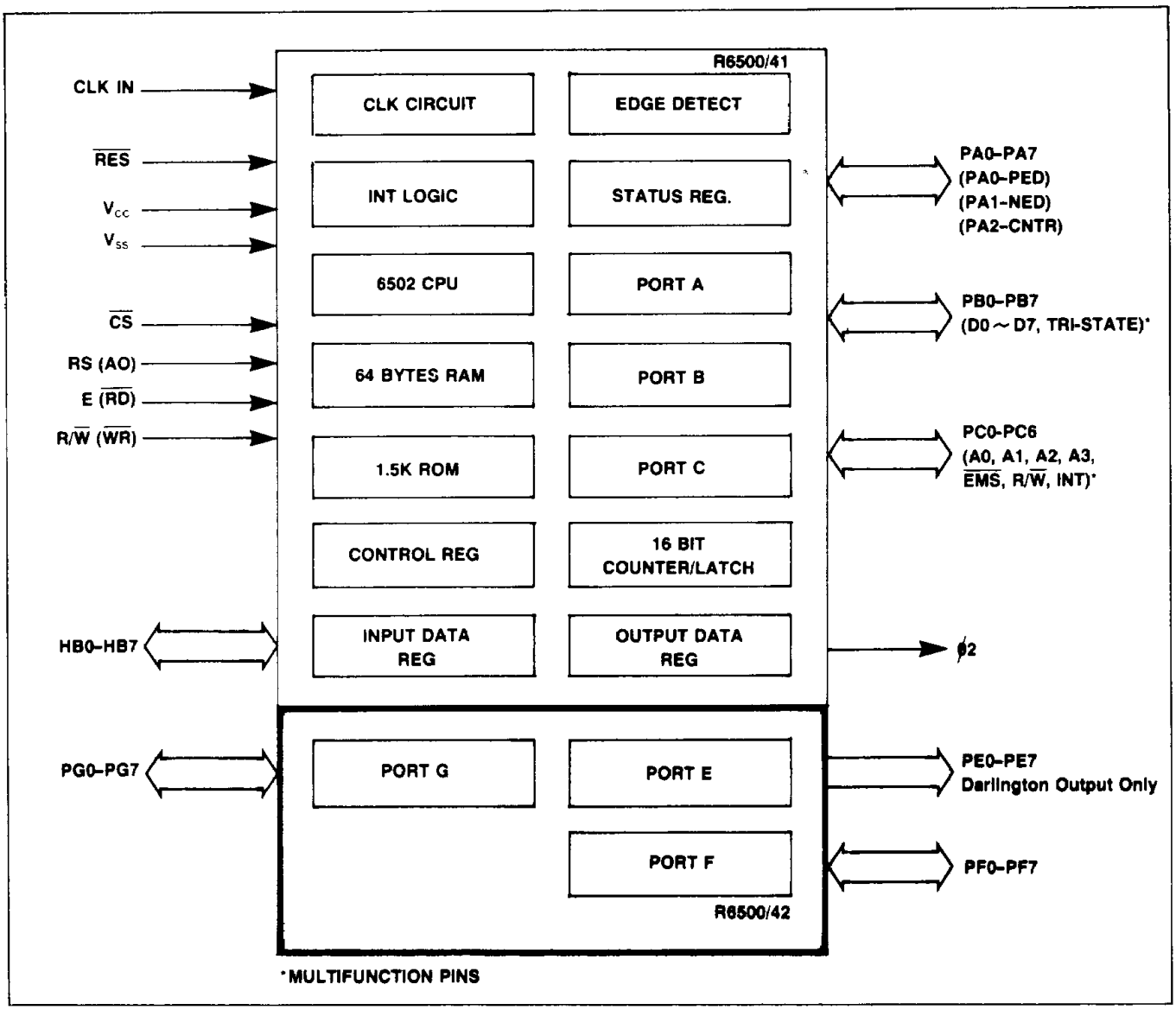


Figure 2-1. Interface Diagram

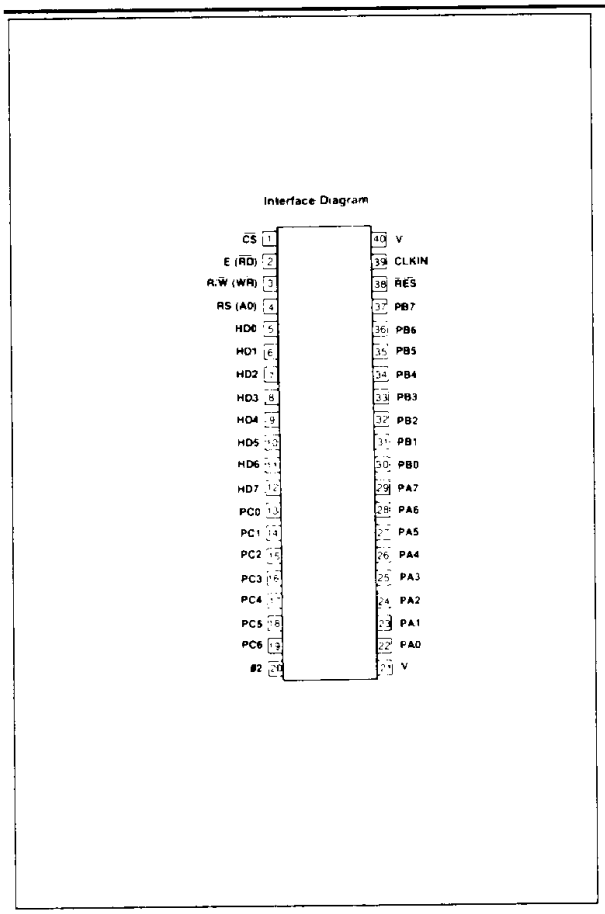


Figure 2.2 R6500/41 Pin Out Designation (40 PIN DIP)

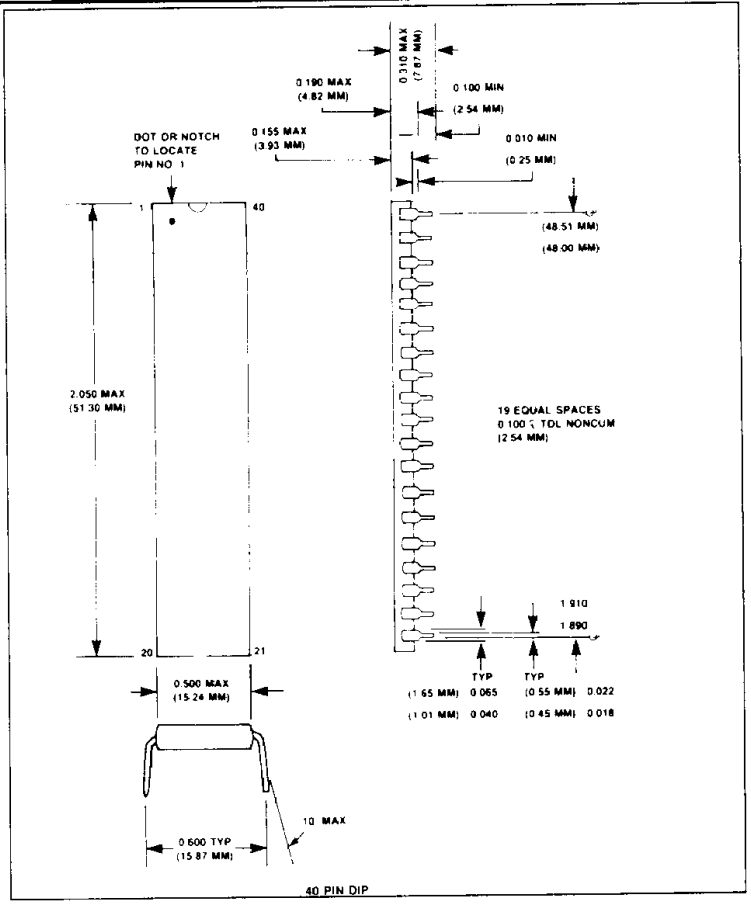


Figure 2-3. R6500/41 Dimensional Outline

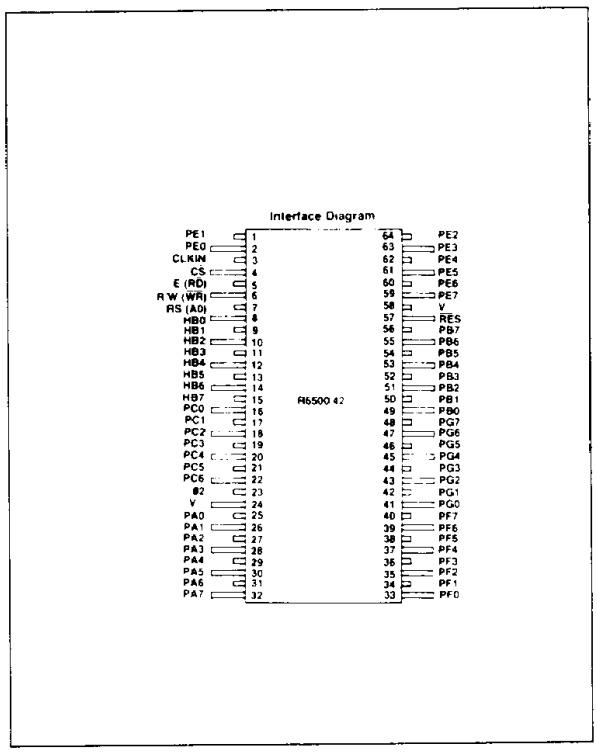


Figure 2-4. R6500/42 Pin Out Designation (64 PIN QUIP)

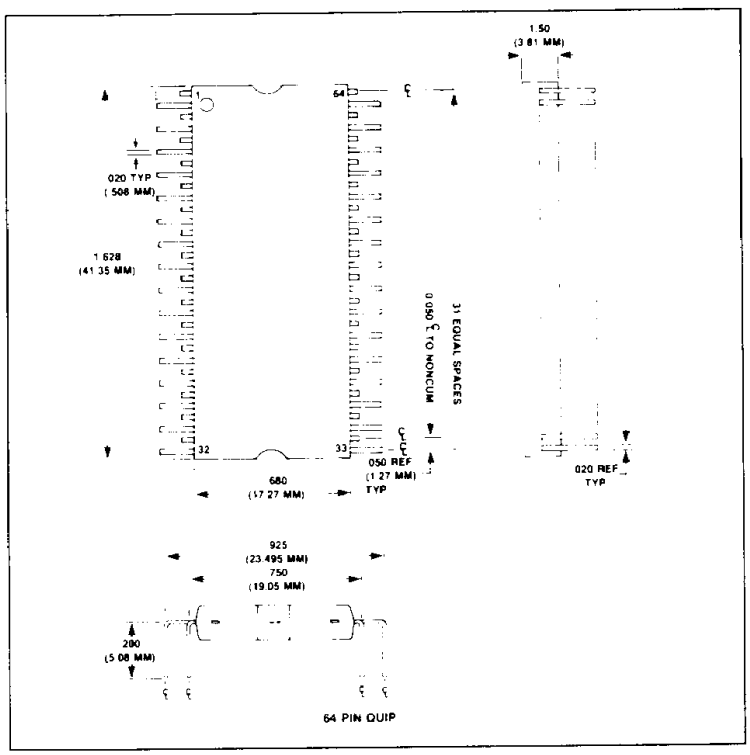


Figure 2-5. R6500/42 Dimensional Outline

Table 2-1. Pin Description

SIGNAL NAME	PIN NO. R6500/41	PIN NO. R6500/42	DESCRIPTION
CLKIN	39	3	Symmetrical square wave 100 KHz to 2 MHZ, TTL compatible input.
$\phi 2$	20	23	Output timing signal—This is an internally synchronized 1 · clock output suitable for external memory or peripheral interfacing.
$\overline{RES}$	38	57	The reset input is used to initialize the device. Section 7 describes the process and conditions of the $\overline{RES}$ procedure.
VCC	40	58	Power supply input (+5V)
VSS	21	24	Signal and power ground (OV).
$\overline{CS}$	1	4	Chip select pin.
RS (A0)	4	7	Register select input pin used by the Host processor to indicate that information being written into the IPC is a data or command byte or to indicate that information being read from the IPC is a status or data byte.
E ($\overline{RD}$)	2	5	Host timing control signal for data register write and read.
R/$\overline{W}$ ($\overline{WR}$)	3	6	Host timing control signal for data register write and read.
HB0-HB7	5-12	8-15	Data bus between Host and IPC data input and output registers.

SIGNAL NAME	PIN NO. R6500/41	PIN NO. R6500/42	DESCRIPTION
PA0-PA7	22-29	25-32	8 bit I/O port used for either input or output. Each line consists of an active transistor to V_{SS} and an optional passive pull-up to V_{CC}. The two lower bits PA0 and PA1 also serve as edge detect inputs. PA2 is time shared with the 16 bit Counter Input or output pin, CNTR, and is mode selected.
PB0-PB7	30-37	49-56	8 bit I/O port used for either input or output. Each line consists of an active transistor to V_{SS} and an active pull-up to V_{CC}. This port becomes a tri-state data bus, D0-D7, in the Abbreviated or Multiplexed Bus Mode. D0-D7 are multiplexed with address lines A4-A11 in the Multiplexed Bus Mode.
PC0-PC6	13-19	16-22	7 bit I/O port used for either input or output. Each line consists of an active transistor to V_{SS} and an optional passive pull-up to V_{CC}. The pins PC0 to PC5 are multiplexed with address and control signals for use in abbreviated and multiplex modes. PC6 is multiplexed with $\overline{INT}$ and is program selectable. In these two modes PC0-PC5 have active pull-ups.
PE0-PE7	N/A	1, 2, 64-59	For the R6500/42, the 64 pin QUIP version, three additional ports (24 lines) are provided. Each line consists of an active transistor to V_{SS}. PF0-PF7 and PG0-PG7 are bidirectional, and an optional passive pull-up to V_{CC} is provided. PE0-PE7 is outputs only with an active pullup. All ports will source 100 μamps. at 2.4v except port E (PE0-PE7) which will source 1 ma. at 1.5v.
PF0-PF7	N/A	33-40	
PG0-PG7	N/A	41-48	

SECTION 3
SYSTEM ARCHITECTURE

This section provides a functional description of the IPC device. Functionally, the device consists of a CPU, both ROM and RAM memories, three parallel I/O ports (six in the 64-pin R6500/42), counter/latch circuit, a mode control register, and an interrupt flag/enable dual register circuit. A block diagram of the system is shown in Figure 3-1.

NOTE

Throughout this document, unless specified otherwise, all memory or register address locations are specified in hexadecimal notation.

3.1 CPU LOGIC

The internal CPU of the device is an enhanced R6502 configuration with an 8-bit Accumulator register, two 8-bit Index Registers (X and Y); an 8-bit Stack Pointer register, an ALU, a 16-bit Program Counter, and standard instruction register/decode and internal timing control logic.

3.1.1 Accumulator

The accumulator is a general purpose 8-bit register that stores the results of most arithmetic and logic operations. In addition, the accumulator usually contains one of the two data words used in these operations.

3.1.2 Index Registers

There are two 8-bit index registers, X and Y. Each index register can be used as a base to modify the address data program counter and thus obtain a new address—the sum of the program counter contents and the index register contents.

When executing an instruction which specifies indirect addressing, the CPU fetches the op code and the address, and modifies the address from memory by adding the index register to it prior to loading or storing the value of memory.

Indexing greatly simplifies many types of programs, especially those using data tables.

3.1.3 Stack Pointer

The Stack Pointer is an 8-bit register. It is automatically incremented and decremented under control of the microprocessor to perform stack manipulation in response to either user instructions, or an internal $\overline{IRQ}$ interrupt. The Stack Pointer must be initialized by the user program.

The stack allows simple implementation of multiple level interrupts, subroutine nesting and simplification of many types of data manipulation. The JSR, BRK, RTI and RTS instructions use the stack and Stack Pointer.

The stack can be envisioned as a deck of cards which may only be accessed from the top. The address of a memory location is stored (or "pushed") onto the stack. Each time data are to be pushed onto the stack, the Stack Pointer is placed on the Address Bus, data are written into the memory location addressed by the Stack Pointer, and the Stack Pointer is decremented by 1. Each time data are read (or "pulled") from the stack, the Stack Pointer is incremented by 1. The Stack Pointer is then placed on the Address Bus, and data are read from the memory location addressed by the Pointer.

The stack is located on zero page, i.e., memory locations 007F-0040. Normal usage calls for the initialization of the Stack Pointer at 007F.

3.1.4 Arithmetic and Logic Unit (ALU)

All arithmetic and logic operations take place in the ALU, including incrementing and decrementing internal registers (except the Program Counter). The ALU cannot store data for more than one cycle. If data are placed on the inputs to the ALU at the beginning of a cycle, the result is always gated into one of the storage registers or to external memory during the next cycle.

Each bit of the ALU has two inputs. These inputs can be tied to various internal buses or to a logic zero; the ALU then generates the function (AND, OR, SUM, and so on) using the data on the two inputs.

3.1.5 Program Counter

The 16-bit Program Counter provides the addresses that are used to step the processor through sequential instructions in a program. Each time the processor fetches an instruction from program memory, the lower (least significant) byte of the Program Counter (PCL) is placed on the low-order bits of the Address Bus and the higher (most significant) byte of the Program Counter (PCH) is placed on the high-order 8 bits of the Address Bus. The Counter is incremented each time an instruction or data is fetched from program memory.

3.1.6 Instruction Register and Instruction Decode

Instructions are fetched from ROM or RAM and gated onto the Internal Data Bus. These instructions are latched into the Instruction Register then decoded along with timing and interrupt signals to generate control signals for the various registers.

3.1.7 Timing Control

The Timing Control Logic keeps track of the specific instruction cycle being executed. This logic is initialized each time an instruction fetch is executed and is advanced at the beginning of each low level of the Clock In pulse for as many cycles as are required to complete the instruction. Each data transfer which takes place between the registers is caused by decoding the contents of both the instruction register and timing control unit.

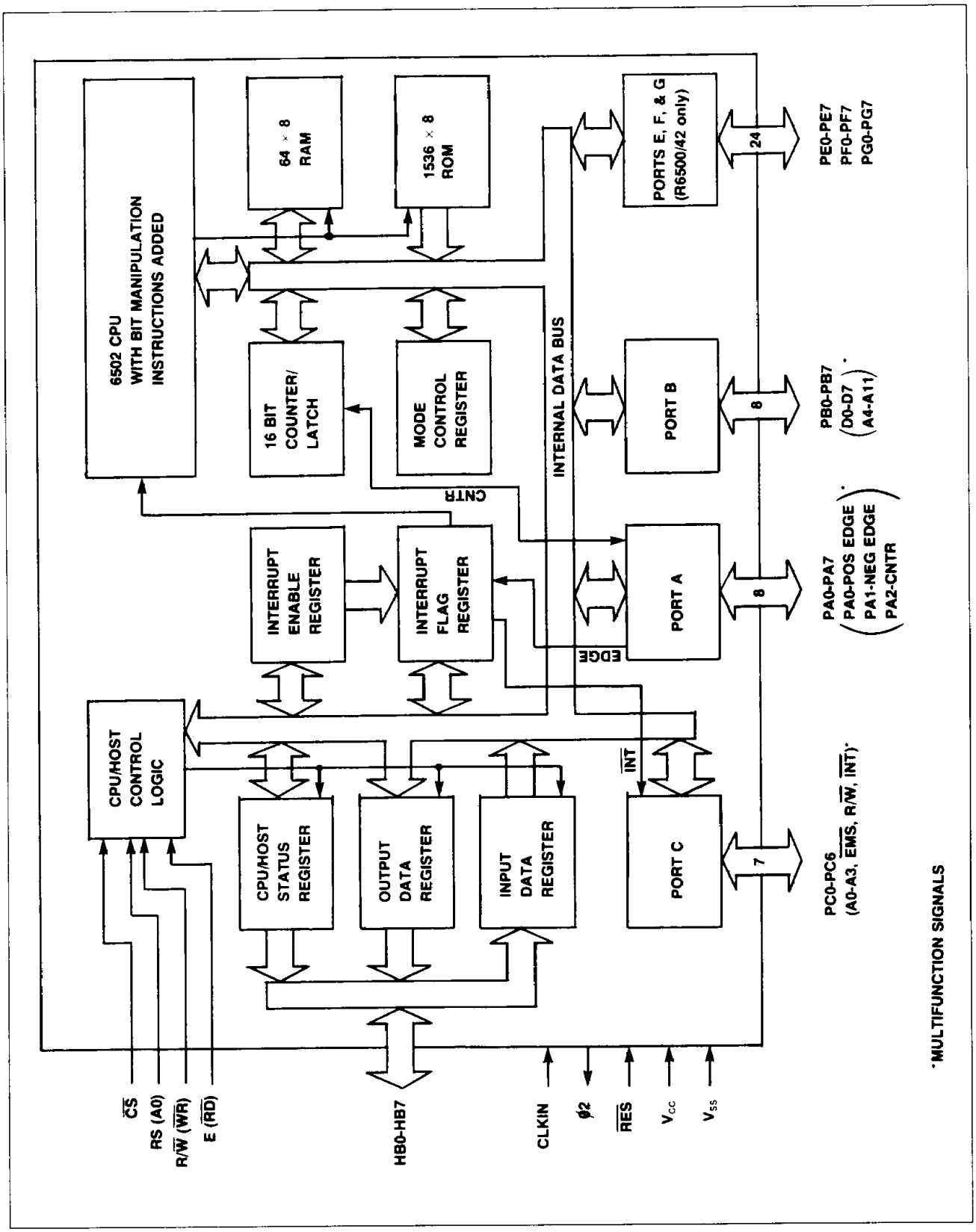


Figure 3-1. R6500/41 & R6500/42 Block Diagram

3.1.8 Interrupt Logic

Interrupt logic controls the sequencing of two interrupts: $\overline{RES}$ and $\overline{IRQ}$. $\overline{IRQ}$ is generated by any one of four conditions: Counter Overflow, Positive Edge Detect, Negative Edge Detect, and Input Data Register Full.

3.2 NEW INSTRUCTIONS

In addition to the standard 6502 instruction set, four instructions have been added to the devices to simplify operations that previously required a read/modify/write operation. In order for these instructions to be equally applicable to any I/O ports, with or without mixed input and output functions, the I/O ports have been designed to read the contents of the specified port data register during the Read cycle of the read/modify/write operation, rather than I/O pins as in normal read cycles. The added instructions and their format are explained in the following subparagraphs. Refer to Appendix A for the Op Code mnemonic addressing matrix for these added instructions.

3.2.1 Set Memory Bit (SMB m, Addr.)

This instruction sets to "1" one of the 8-bit data field specified by the zero page address (memory or I/O port). The first byte of the instruction specifies the SMB operation and 1 of 8 bits to be set. The second byte of the instruction designates address (00-FF) of the byte or I/O port to be operated upon.

3.2.2 Reset Memory Bit (RMB m, Addr.)

This instruction is the same operation and format as SMB instruction except a reset to "0" of the bit results.

3.2.3 Branch on Bit Set Relative (BBS m, Addr, DEST)

This instruction tests one of 8 bits designated by a three bit immediate field within the first byte of the instruction. The second byte is used to designate the address of the byte to be tested within the zero page address range (memory or I/O ports). The third byte of the instruction is used to specify the 8 bit relative address to which the instruction branches if the bit tested is a "1". If the bit tested is not set, the next sequential instruction is executed.

3.2.4 Branch On Bit Reset Relative (BBR m, Addr, DEST)

This instruction is the same operation and format as the BBS instruction except that a branch takes place if the bit tested is a "0".

3.3 READ-ONLY-MEMORY (ROM)

The ROM consists of 1536 bytes (1.5K) mask programmable memory with an address space from FAOO to FFFF. ROM locations FFFC through FFFF are assigned for interrupt and reset vectors.

3.4 RANDOM ACCESS MEMORY (RAM)

The RAM consists of 64 bytes of read/write memory with an assigned page zero address of 0040 through 007F.

3.5 SYSTEM CLOCK

The device functions with an external clock. It is fully asynchronous in reference to the Host computer timing. The device clock frequency equals the external clock frequency. It is also made available for any external device synchronization at pin $\phi 2$.

3.6 MODE CONTROL REGISTER (MCR)

The Mode Control Register contains control bits for the multifunction I/O ports and mode select bits for the Counter, the 6500 or 8080 Bus Select, and the Interrupt ($\overline{INT}$). Its setting determines the basic configuration of the device in any application. Initializing this register is one of the first actions of any software program. The Mode Control Register bit assignment is shown in Figure 3-2.

The use of Counter A Mode Select is shown in Section 6.

The use of the 6500/8080 Host Bus Select is shown in Section 6.

The use of Interrupt Select is shown in Section 4.5.

The use of Bus Mode Select is shown in Sections 4.4 and 4.5.

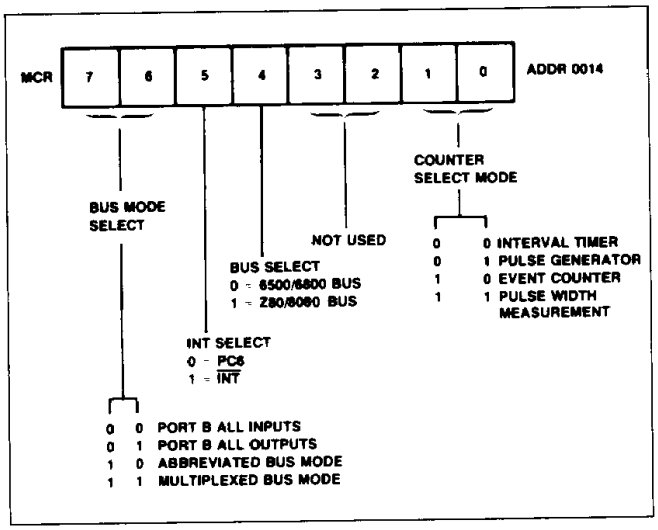


Figure 3-2. Mode Control Register Bit Allocations

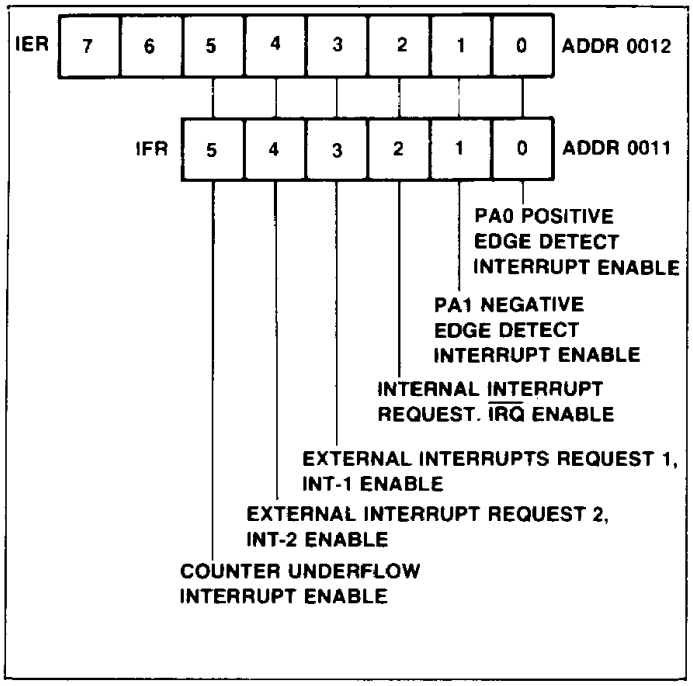


Figure 3-3. Interrupt Enable and Flag Registers

Table 3-1. Interrupt Enable Signals

Control Signal	Description
IER 0	Positive Edge Detect, Interrupt Enable—when this bit is true, a positive going signal on PA0 will generate an $\overline{IRQ}$ and set the corresponding flag bit.
IER 1	Negative Edge Detect Interrupt Enable—when this bit is set to a "1" a negative going signal on PA1 will generate an $\overline{IRQ}$ and set the corresponding flag bit.
IER 2	Input Data Register Full Interrupt Enable—setting this bit to a "1" allows an $\overline{IRQ}$ to be generated each time the Host fills the IDR setting the IDFR bit.
IER 3	Output Data Register Full Interrupt Enable—when this bit is an interrupt request to the Host is generated each time the ODRF flag is set to a "1". (See External Interrupts, Paragraph 3.7.1). Reading the ODR clears INT-1 and ODRF flags.
IER 4	Input Data Register Empty Interrupt Enable—when this is set to a "1" an interrupt is generated to the Host each time the IDR is read by the CPU. The interrupt occurs when the IDRF flag is cleared. INT-2 is cleared when the Host reads the status flag register. (See External Interrupts, Paragraph 3.7.1).
IER 5	Counter Interrupt Enable—if enabled, an $\overline{IRQ}$ is generated whenever the Counter overflows.

3.7 INTERRUPT FLAG REGISTER (IFR) AND INTERRUPT ENABLE REGISTER (IER)

An $\overline{IRQ}$ interrupt request can be initiated by any or all of four possible sources. These sources are all capable of being enabled or disabled by the use of the appropriate interrupt enabled bits in the Interrupt Enable Register (IER). Multiple simultaneous interrupts will cause the $\overline{IRQ}$ interrupt request to remain active until all interrupting conditions have been serviced and cleared.

The Interrupt Flag Register contains the information that indicates which I/O or counter needs attention. The contents of the Interrupt Flag Register may be examined at any time by reading at address: 0011. Edge detect IFR bits may be cleared by executing a RMB instruction at address location 0010. The RMB X, (0010) instruction reads FF, modifies bit X to a "0", and writes the modified value at address location 0011. In this way IFR bits set to a "1" after the read cycle of a Read-Modify-Write instruction (such as RMB) are protected from being cleared. IFR bits 6 and 7 are indeterminate on a Read.

Each IFR bit has a corresponding bit in the Interrupt Enable Register which can be set to a "1" by writing a "1" in the respective bit position at location 0012. Individual IER bits may be cleared by writing a "0" in the respective bit position, or by $\overline{RES}$. If set to a "1", an $\overline{IRQ}$ will be generated when the corresponding IFR bit becomes true. The Interrupt Flag Register and Interrupt Enable Register bit assignments are shown in Figure 3-3 and the functions of each bit are explained in Table 3-1.

3.7.1 External Interrupts ($\overline{INT}$)

An external interrupt $\overline{INT}$ to the Host computer may be selected in two modes. (See Section 5 for information on the Host/Device interface).

OUTPUT DATA REGISTER (ODR) FULL

When IER 3 of the Interrupt Enable Register is set to a "1", the device will assert the $\overline{INT}$ (PC6) line each time it loads the ODR. The ODRF flag of the Status Flag Register and the IFR 3 of the IFR will be set to a "1" indicating the ODR is full. The ODRF and IFR 3 flags are cleared and $\overline{INT}$ is negated when the Host processor reads the ODR.

INPUT DATA REGISTER (IDR) EMPTY

When IER 4 of the Interrupt Enable Register is set to a "1", the device will assert the $\overline{INT}$ (PC6) line each time it reads the IDR. The IDRF flag of the Host Status Flag Register will be cleared and the IFR 4 flag of the IFR will be set to a "1" indicating the IDR has just been read by the device. The IFR 4 flag is cleared and $\overline{INT}$ is negated when the Host processor reads the Host Status Flag Register. $\overline{RES}$ clears the IDR and sets the IFR4 flag to indicate the register is empty.

3.8 PROCESSOR STATUS REGISTER

The 8-bit Processor Status Register, shown in Figure 3-4, contains seven status flags. Some of these flags are controlled by the user program; others may be controlled both by the user's program and the CPU. The R6502 instruction set contains a number of conditional branch instructions which are designed to allow testing of these flags. Each of the eight processor status flags is described in the following sections.

3.8.1 Carry Bit (C)

The Carry Bit (C) can be considered as the ninth bit of an arithmetic operation. It is set to logic 1 if a carry from the eighth bit has occurred or cleared to logic 0 if no carry occurred as the result of arithmetic operations.

The Carry Bit may be set or cleared under program control by use of the Set Carry (SEC) or Clear Carry (CLC) instruction, respectively. Other operations which affect the Carry Bit are ADC, ASL, CMP, CPX, CPY, LSR, PLP, ROL, ROR, RTI, and SBC.

3.8.2 Zero Bit (Z)

The Zero Bit (Z) is set to logic 1 by the CPU during any data movement or calculation which sets all 8 bits of the result to zero. This bit is cleared to logic 0 when the resultant 8 bits of a data movement or calculation operation are not all zero. The R6502 instruction set contains no instruction to specifically set or clear the Zero Bit. The Zero Bit is, however, affected by the following instructions; ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TXA, TSX, and TYA.

3.8.3 Interrupt Disable Bit (I)

The Interrupt Disable Bit (I) is used to control the servicing of an interrupt request (IRQ). If the I Bit is reset to logic 0, the $\overline{IRQ}$ signal will be serviced. If the bit is set to logic 1, the $\overline{IRQ}$ signal will be ignored. The CPU will set the Interrupt Disable Bit to logic 1 if a RESET ($\overline{RES}$) or Non-Maskable Interrupt ($\overline{NMI}$) signal is detected.

The I bit is cleared by the Clear Interrupt Mask Instruction (CLI) and is set by the Set Interrupt Mask Instruction (SEI). This bit may also be set by the BRK Instruction. The Return from Interrupt (RTI) and Pull Processor Status (PLP) instructions will also affect the I bit.

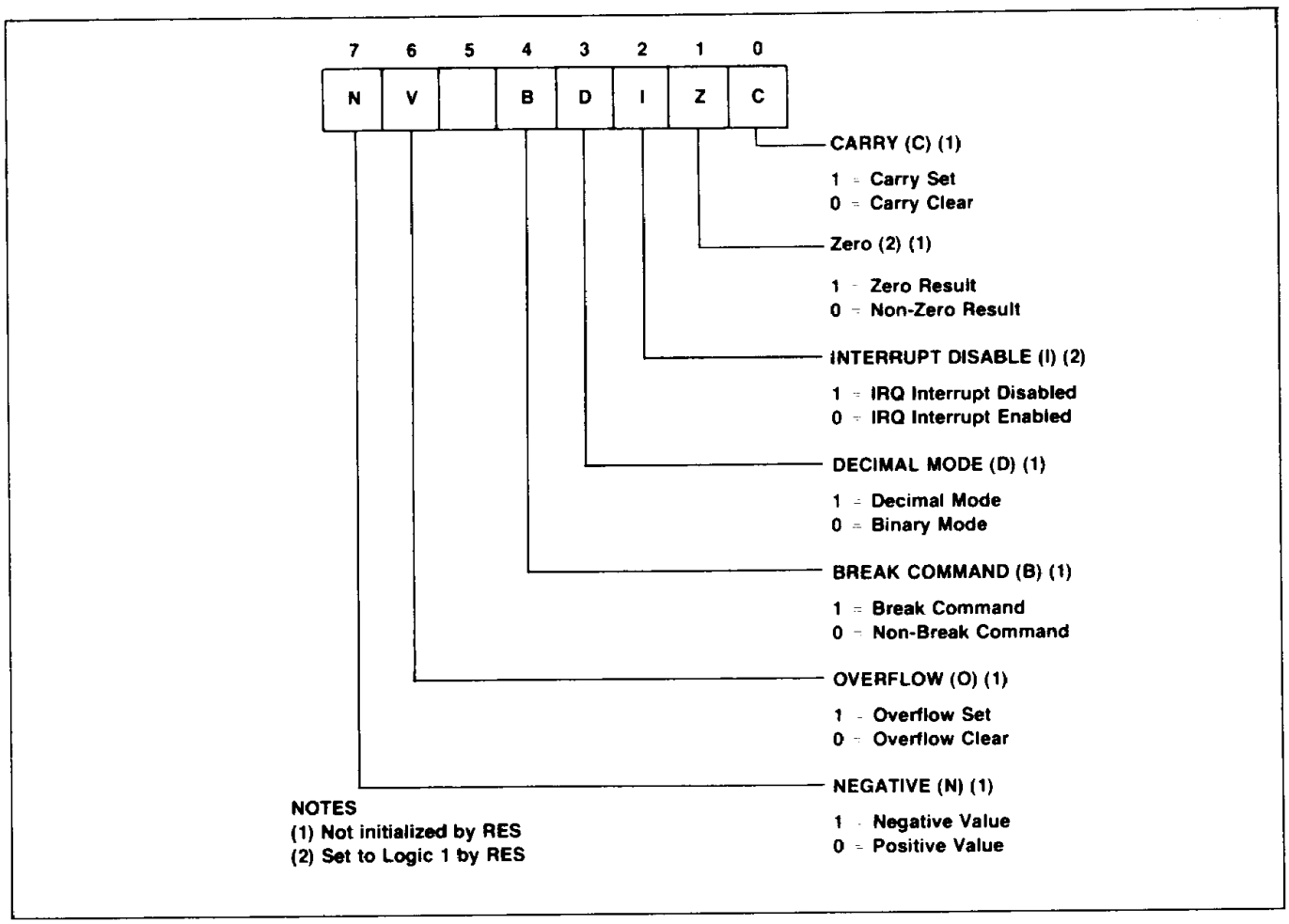


Figure 3-4. Processor Status Register

3.8.4 Decimal Mode Bit (D)

The Decimal Mode Bit (D), is used to control the arithmetic mode of the CPU. When this bit is set to logic 1, the adder operates as a decimal adder. When this bit is cleared to logic 0, the adder operates as a straight binary adder. The adder mode is controlled only by the programmer. The Set Decimal Mode (SED) instruction will set the D bit; the Clear Decimal Mode (CLD) instruction will clear it. The PLP and RTI instructions also effect the Decimal Mode Bit.

CAUTION

The Decimal Mode Bit will either set or clear in an unpredictable manner upon power application to the device. This bit must be initialized to the desired state by the user program or erroneous results may occur.

3.8.5 Break Bit (B)

The Break Bit (B) is used to determine the condition which caused the $\overline{IRQ}$ service routine to be entered. If the $\overline{IRQ}$ service routine was entered because the CPU executed a BRK command, the Break Bit will be set to logic 1. If the $\overline{IRQ}$ routine was entered as the result of an $\overline{IRQ}$ signal being generated, the B bit will be cleared to logic 0. There are no instructions which can set or clear this bit.

3.8.6 Overflow Bit (V)

The Overflow Bit (V) is used to indicate that the result of a signed, binary addition, or subtraction, operation is a value that cannot be contained in seven bits (- 128 · n · 127). This indicator only has meaning when signed arithmetic (sign and seven magnitude bits) is performed. When the ADC or SBC instruction is performed, the Overflow Bit is set to logic 1 if the polarity of the sign bit (bit 7) is changed because the result exceeds +127 or -128; otherwise the bit is cleared to logic 0. The V bit may also be cleared by the programmer using a Clear Overflow (CLV) instruction.

The Overflow Bit may also be used with the BIT instruction. The BIT instruction which may be used to sample interface devices, allows the overflow flag to reflect the condition of bit 6 in the sampled field. During a BIT instruction the Overflow Bit is set equal to the content of the bit 6 on the data tested with BIT instrction. When used in this mode, the overflow has nothing to do with signed arithmetic, but is just another sense bit for the microprocessor. Instructions which affect the V flag are ADC, BIT, CLV, PLP, RTI and SBC.

3.8.7 Negative Bit (N)

The Negative Bit (N) is used to indicate that the sign bit (bit 7), in the resulting value of a data movement or data arithmetic operation, is set to logic 1. If the sign bit is set to logic 1, the resulting value of the data movement or arithmetic operation is negative; if the sign bit is cleared, the result of the data movement or arithmetic operation is positive. There are no instructions that set or clear the Negative Bit since the Negative Bit represents only the status of a result. The instructions that effect the state of the Negative Bit are: ADC, AND, ASL, BIT, CMP, CPX, CPY, DEC, DEX, DEY, EOR, INC, INX, INY, LDA, LDX, LDY, LSR, ORA, PLA, PLP, ROL, ROR, RTI, SBC, TAX, TAY, TSX, TXA, and TYA.

SECTION 4
PARALLEL INPUT/OUTPUT PORTS

INPUT/OUTPUT PORTS

The IPC device provides three ports (PA, PB, and PC). The 15 lines of PA and PC are completely bidirectional, that is, there are no line grouping or port association restrictions. The eight lines of Port B may be programmed as all inputs or all outputs. Port PC, however, may be multiplexed under program control with seven other signals. Six of these signals form an address and control bus for extended addressing. The seventh signal is multiplexed with an external interrupt output, $\overline{INT}$. All eight Port B lines are tri-state to permit their use as a data bus during extended addressing modes.

The R6500/42, a 64 pin QUIP device, has three additional ports: PE, PF, and PG. PE is outputs only. PF and PG are bidirectional.

Internal pull-up resistors (FET's with an impedance range of 3K $\leq$ Rpu $\leq$ 12K ohm) may be provided on ports PA and PC and ports PF & PG (R6500/42 only), as a mask option.

The direction of the I/O lines are controlled by 8-bit port registers located in page zero. This arrangement provides quick programming access using simple two-byte zero page address instructions. There are no direction registers associated with the I/O ports, which simplifies I/O handling. The I/O addresses are shown in Table 4-1. Section E.6 shows the I/O Port Timing.

Table 4-1. I/O Port Addresses

PORT		ADDRESS
A		0000
B		0001
C		0002
E	R6500/42 only	0004
F	R6500/42 only	0005
G	R6500/42 only	0006

4.1 INPUTS

Inputs for Ports A and C, and also Ports F and G of the R6500/42, are enabled by loading logic 1 into all I/O port register bit positions that are to correspond to I/O input lines. A low (<0.8V) input signal will cause a logic 0 to be read when a read instruction is issued to the port register. A high (>2.0V) input will cause a logic 1 to be read. An $\overline{RES}$ signal forces all I/O port registers to logic 1 thus initially treating all I/O lines as inputs.

Port B may be all inputs or all outputs. All inputs is selected by setting bits MCR6 and MCR7 of the Mode Control Register to a "0".

The status of the input lines can be interrogated at any time by reading the I/O port addresses. Note that this will return the actual status of the input lines, not the data written into the I/O port registers.

Read/Modify/Write instructions can be used to modify the operation of PA, PB, PC, and also PF, & PG of the R6500/42. During the Read cycle of a Read/Modify/Write instruction the Port I/O register is read. For all other read instructions the port input lines are read. Read/Modify/Write instructions are: ASL, BBS, BBR, DEC, INC, LSR, RMB, ROL, ROR, and SMB.

4.2 OUTPUTS

Outputs for Ports A thru C, and Ports E thru G of the R6500/42, are controlled by writing the desired I/O line output states into the corresponding I/O port register bit positions. A logic 1 will force a high (>2.4V) output while a logic 0 will force a low (<0.4V) output. Port B also requires that MCR6 be set to a "1" and MCR7 be set to a "0".

4.3 PORT A (PA)

Port A can be programmed via the Mode Control Register (MCR) as a standard parallel 8-bit, bit independent, I/O port, or a counter I/O line. Table 4-2 tabulates the control and usage of Port A.

In addition to their normal I/O functions, PA0 can detect positive going edges, and PA1 can detect negative going edges. An edge transition on these pins will set a corresponding status bit in the IFR and generate an interrupt request if the respective Interrupt Enable Bit is set. The maximum rate at which an edge can be detected is one-half the $\phi 2$ clock rate. Edge detection timing is shown in Section E.5.

Table 4-2. Port A Control & Usage

PA0-PA1 I/O		PA2 I/O		PA2 COUNTER				PA3-PA7 I/O	
		MCR0 = 0 MCR1 = 0		MCR0 = 1 MCR1 = 0		MCR0 = X MCR1 = 1			
SIGNAL		SIGNAL		SIGNAL		SIGNAL		SIGNAL	
NAME	TYPE	NAME	TYPE	NAME	TYPE	NAME	TYPE	NAME	TYPE
PA0 (1) PA1(2)	I/O I/O	PA2	I/O	CNTR	OUTPUT	CNTR	INPUT (3)	PA3-PA7	I/O

(1) POSITIVE EDGE DETECT (2) NEGATIVE EDGE DETECT (3) HARDWARE BUFFER FLOAT

4.4 PORT B (PB)

Port B can be programmed as an I/O Port, an 8-bit tri-state data bus, or as a multiplexed bus. Mode selection for Port B is made by the Mode Control Register (MCR). The Port B output drivers can be selected as tri-state output drivers by setting bit 7 of the MCR to 0 (zero) and bit 6 of the MCR to 1. An all inputs condition is created by setting both MCR6 and MCR7 to 0 (zero). Table 4-3 shows the necessary settings for the MCR to achieve the various modes for Port B. When Port B is selected to operate in the Abbreviated Mode PB0-PB7 serves as data register bits D0-D7. When Port B is selected to operate in the Multiplexed Mode data bits D0 through D7 are time multiplexed with address bits A4 through A11, respectively. Refer to the Memory Maps (Appendix B) for Abbreviated and Multiplexed memory assignments. See Appendix E.3 through E.5 for Port B timing.

4.5 PORT C (PC)

Port C can be programmed as an I/O port and in conjunction with Port B, as an abbreviated bus, or as a multiplexed bus. When used in the abbreviated or multiplexed bus modes, PC0-PC5 function as A0-A3, R/W, and $\overline{EMS}$, respectively, as shown in Table 4-4. $\overline{EMS}$ (External Memory Select) is asserted (low) whenever the internal processor accesses memory area between 0080 and 0FFF. (See Memory Map, Appendix C). The leading edge of $\overline{EMS}$ may be used to strobe the eight address lines multiplexed on Port B in the Multiplexed Bus Mode. See Appendix E.3 through E.5 for Port C timing.

4.6 PORT E, PORT F AND PORT G (PE, PF & PG) R6500/42 ONLY

Port E only operates in the Output mode. It provides a Darlington output that can source current at the high (1) level. Port F and Port G operate identically and can be programmed as bidirectional I/O ports. They have standard output capability. See Appendix E.3 through E.5 for Port E, F & Port G timing.

Table 4-3. Port B Control & Usage

R6500/41 PIN #	R6500/42 PIN #	I/O MODES MCR7 = 0 MCR6 = 0 SIGNAL NAME	TYPE (1)	I/O MODES MCR7 = 0 MCR6 = 1 SIGNAL NAME	TYPE (2)	ABBREVIATED MODE MCR7 = 1 MCR6 = 0 SIGNAL NAME	TYPE (3)	MULTIPLEXED MODE MCR7 = 1 MCR6 = 1 PHASE 1 SIGNAL NAME	TYPE (2)	PHASE 2 SIGNAL NAME	TYPE (3)
30	49	PB0	INPUT	PB0	OUTPUT	D0	I/O	A4	OUTPUT	D0	I/O
31	50	PB1	INPUT	PB1	OUTPUT	D1	I/O	A5	OUTPUT	D1	I/O
32	51	PB2	INPUT	PB2	OUTPUT	D2	I/O	A6	OUTPUT	D2	I/O
33	52	PB3	INPUT	PB3	OUTPUT	D3	I/O	A7	OUTPUT	D3	I/O
34	53	PB4	INPUT	PB4	OUTPUT	D4	I/O	A8	OUTPUT	D4	I/O
35	54	PB5	INPUT	PB5	OUTPUT	D5	I/O	A9	OUTPUT	D5	I/O
36	55	PB6	INPUT	PB6	OUTPUT	D6	I/O	A10	OUTPUT	D6	I/O
37	56	PB7	INPUT	PB7	OUTPUT	D7	I/O	A11	OUTPUT	D7	I/O

(1) TRI-STATE BUFFER IS IN HIGH IMPEDANCE MODE (2) TRI-STATE BUFFER IS IN ACTIVE MODE
(3) TRI-STATE BUFFER IS IN ACTIVE MODE ONLY DURING THE PHASE 2 PORTION OF A WRITE CYCLE

Table 4-4. Port C Control & Usage

R6500/41 PIN #	R6500/42 PIN #	I/O MODE MCR7 = 0 MCR6 = X SIGNAL NAME	TYPE (1)	ABBREVIATED MODE MCR7 = 1 MCR6 = 0 SIGNAL NAME	TYPE (2)	MULTIPLEXED MODE MCR7 = 1 MCR6 = 1 SIGNAL NAME	TYPE (2)
13	16	PC0	I/O	A0	OUTPUT	A0	OUTPUT
14	17	PC1	I/O	A1	OUTPUT	A1	OUTPUT
15	18	PC2	I/O	A2	OUTPUT	A2	OUTPUT
16	19	PC3	I/O	A3	OUTPUT	A3	OUTPUT
17	20	PC4	I/O	$\overline{EMS}$	OUTPUT	$\overline{EMS}$	OUTPUT
18	21	PC5	I/O	R/$\overline{W}$	OUTPUT	R/$\overline{W}$	OUTPUT
19	22	PC6*	I/O	$\overline{INT}$*	OUTPUT	$\overline{INT}$*	OUTPUT

(1) RESISTIVE PULL-UP, ACTIVE BUFFER PULL-DOWN
(2) ACTIVE BUFFER PULL-UP AND PULL-DOWN
*PC6 if MCR5 = 0; $\overline{INT}$ if MCR5 = 1

SECTION 5
HOST INTERFACE BUS

Two way data transfers are performed between the IPC and the Host microprocessor by means of the Output Data Register and the Input Data Register. The Host can also write a command to the IDR and read from the Host Status Flag Register. Table 5-1 shows the Host addressing matrix. A hardware interrupt procedure and a software polling procedure is available to control data traffic between the CPU and Host.

Table 5-1. Host Addressing Matrix

RS (A_0)	READ	WRITE
1	HOST STATUS FLAG	COMMAND INPUT
0	DATA REG OUTPUT	DATA REG INPUT

5.1 DATA REGISTERS

The device has an 8-bit Input Data Register (IDR) and an 8-bit Output Data Register (ODR). The IDR serves as a temporary storage for commands and data from the Host to the device. When transferring data from the Host to the device, the following conditions are in effect:

- $\overline{CS}$ is asserted
- RS (AO) indicates command input or data input.
- The contents of the host data bus (HB0-HB7) are copied into the IDR when the appropriate Host bus write signals are asserted.

The ODR serves as a temporary storage for data from the device to the Host. When the Host is reading data from the device, the following conditions are in effect:

- $\overline{CS}$ is asserted
- RS (AO) input selects ODR or HSFR
- The contents of ODR or the Flag Register are placed on the host data bus (HB0-HB7) when the appropriate Host read signals are asserted.

5.2 HOST STATUS FLAG REGISTER

A Host Status Flag Register facilitates a software protocol that permits independent and uninterrupted flow of data asynchronously between the host computer and the device.

The Host Status Flag Register contains 8 flag bits that can be read at anytime by either the Host or the device. See Figure 5-1. General purpose flags F2 through F6 are serviced by the device in either read or write modes and monitored by the Host (Read Only).

Flag F1 can be read at anytime by either the host or the device. The F1 flag copies the A0 (RS) input signal during any host write data exchange. The device can write to the F1 flag at any time.

The ODRF (Output Data Register Full) flag is set each time the device writes to the Output Data Register. The setting of the ODRF sets the device Interrupt Status Register IFR3 flag. An Output Interrupt ($\overline{INT}$) may be generated under program control by setting IER3 in the interrupt enable register. The ODRF flag is reset only by a hardware reset or by the host performing a read on the output data register. The ODRF flag is reset following the conclusion of any host output data register read. The resetting of the ODRF causes the reset of the IFR3 flag and thus the reset of the external interrupt ($\overline{INT}$).

The IDRF (Input Data Register Full) flag is set following the conclusion of any host write data exchange. The setting of the IDRF causes IFR2 of the device status register to be set. An internal interrupt may be generated under program control by setting IER2 in the Interrupt Enable Register. The setting of IDRF also causes IFR4 to be reset. The IDRF resets during device read of the input data register. IFR2 sets and IFR4 resets following the reset of IDRF. IFR4 may generate an external output interrupt (INT, input buffer empty), under program control by setting IER4 in the interrupt enable register.

The Host Status Flag Register is cleared by the $\overline{RES}$ input.

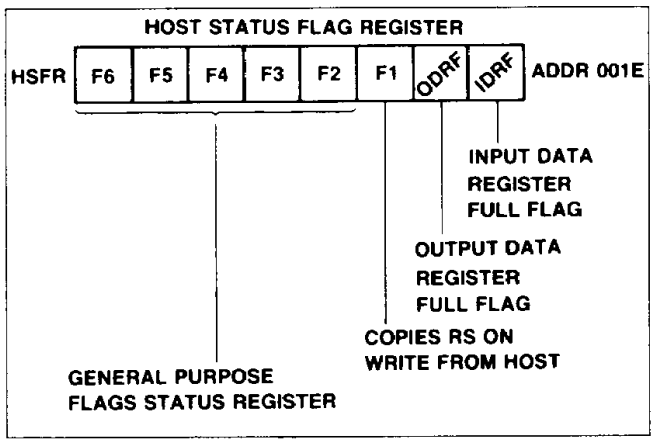


Figure 5-1. Host Status Flag Register Bit Allocation

5.3 HOST COMPUTER INTERFACE

The device will work with a variety of Host Computers. The HOST interface consists of a chip select, one address line, 2 control lines and an 8 bit three state data bus. Internal logic of the device, controlled by MCR4, configures, the address and two control lines to either a 6500 or 8080 operational methodology. The interface is completely asynchronous and will work with a Host Computer up to a 5 MHz bus transfer rate. The device clock input frequency need not be the same as the Host's. A mode control register is set to match the interface to that of the Host device as follows:

MCR4 = 0 When MCR4 is set to a logic zero, the IPC is configured to operate on a 6502/6800 type host bus. In this mode, the E input is connected to the host transfer strobe (VMA or 02 for 6800, 02 for 6500) and the R/W input is connected to the host microprocessor R/W output line. Figure 5-3 and Table 5-2, together, specify the relevant timing for read and write cycles on this type of host bus.

MCR4 = 1 When MCR4 is set to a logic one, the IPC is configured for operation on an 8080/Z80 type bus. In this mode, the RD input is used as a read strobe and the WR input is connected to the write strobe of the host microprocessor bus. Figure 5-4 and Table 5-3 show the relevant timing characteristics for this mode of operation.

Table 5-2. Host Interface Timing Characteristics BSEL = 0 (6500)

Characteristics 1 and 2 MHz	Symbol	Min	Max
$\overline{CS}$, R/$\overline{W}$, RS Setup Time	t_{CS}	10	—
Access Time	t_{DA}	—	90°
Data Hold Time	t_{DHR}	10	—
Control Hold Time	t_{HC}	10	—
Write Data Setup Time	t_{WDS}	75	—
Write Data Hold Time	t_{DHW}	10	—
Write Stroke Width	t_{WR}	75	—

Note:
90 ns when loading = 130 pF + 1 TTL LOAD and
75 ns when loading = 90 pF + 1 TTL LOAD.

Table 5-3. Host Interface Timing Characteristics BSEL = 1 (8080)

Characteristics 1 and 2 MHz	Symbol	Min	Max
$\overline{CS}$, A0 Setup Time	t_{CS}	10	—
Data Access Time on Read	t_{DA}	—	90°
Data Hold Time	t_{DHR}	10	—
Control Hold Time	t_{HC}	10	—
Write Data Setup Time	t_{WDS}	75	—
Write Data Hold Time	t_{DHW}	10	—
Write Stroke Width	t_{WR}	75	—

Note:
90 ns when loading = 130 pF + 1 TTL LOAD and
75 ns when loading = 90 pF + 1 TTL LOAD.

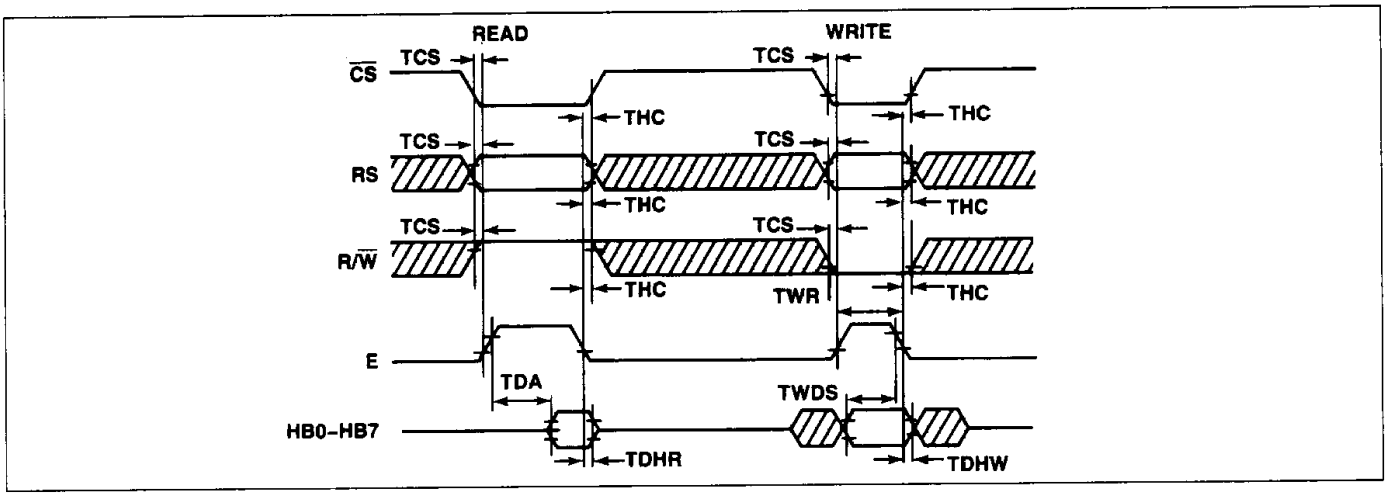


Figure 5-3. Timing Diagram—Host Interface (MCR4 = 0) (6500 Version)

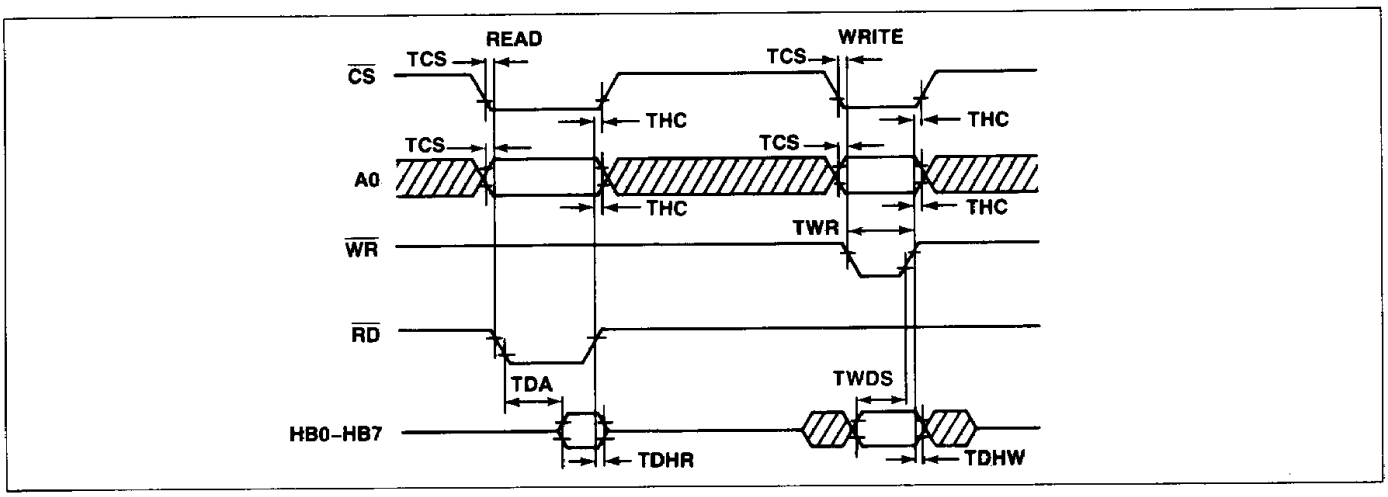


Figure 5-4. Timing Diagram—Host Interface (MCR4 = 1) (8080 Version)

SECTION 6
COUNTER/TIMERS

The device contains a 16-bit counter and a 16-bit latch associated with it. The counter can be independently programmed to operate in one of four modes:

Counter

- Pulse width measurement
- Pulse Generation
- Interval Timer
- Event Counter

Operating modes of the Counter are controlled by the Mode Control Register. All counting begins at the initialization value and decrements. When modes are selected requiring a counter input/output line, PA2 is selected for Counter I/O.

6.1 COUNTER

The Counter consists of a 16-bit counter and a 16-bit latch organized as follows: Lower Counter (LC), Upper Counter (UC), Lower Latch (LL), and Upper Latch (UL). The counter contains the count of either ϕ2 clock pulses or external events, depending on the counter mode selected. The contents of the Counter may be read any time by executing a read at location 0018 for the Upper Counter and at location 001A or location 0019 for the Lower Counter. A read at location 0019 also clears the Counter Underflow Flag (IFR5).

The 16-bit latch contains the counter initialization value, and can be loaded at any time by executing a write to the Upper Latch at location 0018 and the Lower Latch at location 001A. In either case, the contents of the accumulator are copied into the applicable latch register.

The Counter can be started at any time by writing to address 0019. The contents of the accumulator will be copied into the Upper Latch before the contents of the 16-bit latch are transferred to the Counter. The counter is set to the latch value whenever the Counter underflows. When the Counter decrements from 0000 the next counter value will be the latch value, not FFFF, and the Counter Underflow Flag (IFR 5) will be set to "1". This bit may be cleared by reading the Lower Counter at location 0019, by writing to address location 0019, or by $\overline{RES}$.

The Counter operates in any of four modes. These modes are selected by the Counter Mode Control bits in the Control Register.

MCR1 (bit 1)	MCR0 (bit 0)	Mode
0	0	Interval Timer
0	1	Pulse Generation
1	0	Event Counter
1	1	Pulse Width Measurement

The Interval Timer, Pulse Generation, and Pulse Width Measurement Modes are ϕ2 clock counter modes. The Event Counter Mode counts the occurrences of an external event on the CNTR line (PA2).

The Counter is set to the Interval Timer Mode (00) when a $\overline{RES}$ signal is generated.

6.1.1 Interval Timer Mode

In the Interval Timer mode the Counter is initialized to the Latch value by either of two conditions:

1. When the Counter is decremented from 0000, the next Counter value is the Latch value (not FFFF).

2. When a write operation is performed to the Load Upper Latch and Transfer Latch to Counter address 0019, the Counter is loaded with the Latch value. Note that the contents of the Accumulator are loaded into the Upper Latch before the Latch value is transferred to the Counter.

The Counter value is decremented by one count at the ϕ2 clock rate. The 16-bit Counter can hold from 1 to 65535 counts. The Counter Timer capacity is therefore 1μs to 65.535 ms at the 1 MHz ϕ2 clock rate or 0.5μs to 32.767 ms at the 2 MHz ϕ2 clock rate. Time intervals greater than the maximum Counter value can be easily measured by counting $\overline{IRQ}$ interrupt requests in the counter $\overline{IRQ}$ interrupt routine.

When the Counter decrements from 0000, the Counter Underflow (IFR5) is set to logic 1. If the Counter Interrupt Enable Bit (IER5) is also set, an $\overline{IRQ}$ interrupt request will be generated. The Counter Underflow bit in the Interrupt Flag Register can be examined in the $\overline{IRQ}$ interrupt routine to determine that the $\overline{IRQ}$ was generated by the Counter Underflow.

While the timer is operating in the Interval Timer Mode, PA2 operates as a PA I/O.

A timing diagram of the Interval Timer Mode is shown in Figure 6-1.

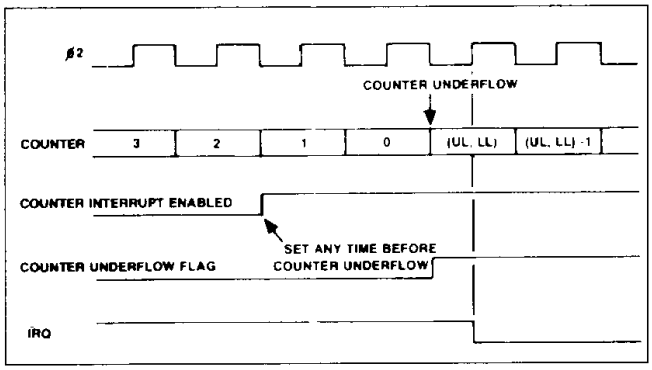


Figure 6-1. Interval Timer Timing Diagram

6.1.2 Pulse Generation Mode

In the Pulse Generation mode, the PA2 line operates as a Counter Output. The line toggles from low to high or from high to low whenever a Counter Underflow occurs, or a write is performed to address 0019.

The normal output waveform is a symmetrical square-wave. The PA2 output is initialized high when entering the mode and transitions low when writing to 0019.

Asymmetric waveforms can be generated if the value of the latch is changed after each counter underflow.

A one-shot waveform can be generated by changing from Pulse Generation to Interval Timer mode after only one occurrence of the output toggle condition.

6.1.3 Event Counter Mode

In this mode PA2 is used as an Event Input line, and the Counter will decrement with each rising edge detected on this line. The maximum rate at which this edge can be detected is one-half the ϕ2 clock rate.

The Counter can count up to 65,535 occurrences before underflowing. As in the other modes, the Counter Underflow bit (IER5) is set to logic 1 if the underflow occurs.

Figure 6.2 is a timing diagram of the Event Counter Mode.

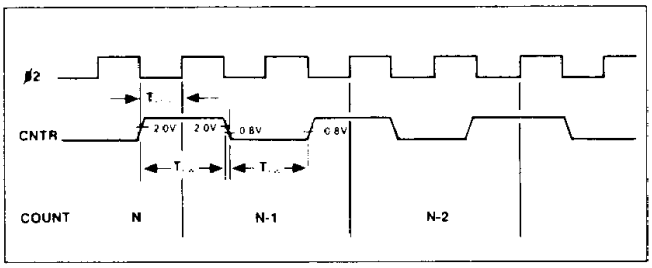
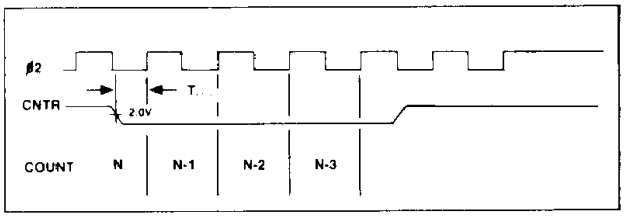


Figure 6-2. Event Counter Mode

6.1.4 Pulse Width Measurement Mode

This mode allows the accurate measurement of a low pulse duration on the PA2 line. The Counter decrements by one count at the ϕ2 clock rate as long as the PA2 line is held in the low state. The Counter is stopped when PA2 is in the high state.

The Counter underflow flag will be set only when the count in the timer reaches zero. Upon reaching zero the timer will be loaded with the latch value and continue counting down as long as the PA2 pin is held low. After the counter is stopped by a high level on PA2, the count will hold as long as PA2 remains high. Any further low levels on PA2 will again cause the counter to count down from its present value. The state of the PA2 line can be determined by testing the state of PA2.



SECTION 7
POWER ON/INITIALIZATION CONSIDERATIONS

7.1 POWER ON TIMING

After application of VCC power to the device, $\overline{RES}$ must be held low for at least eight stable $\phi 2$ clock cycles after V_{CC} reaches operating range.

Figure 7-1 illustrates the power turn-on waveforms. External clock stabilization time is typically 20ms.

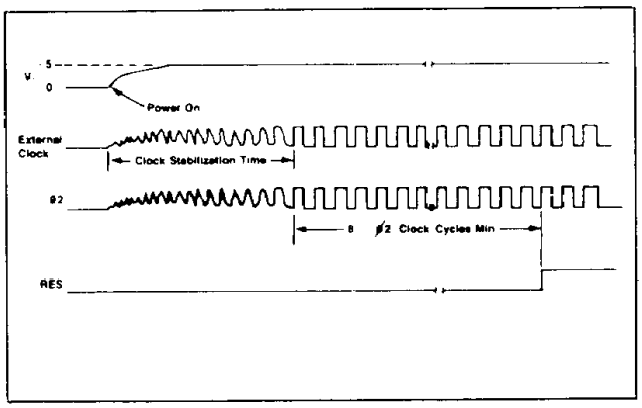


Figure 7-1. Power Turn-On Timing Detail

7.2 POWER-ON RESET

The occurrence of $\overline{RES}$ going from low to high will cause the device to set the Interrupt Mask Bit—bit 2 of the Processor Status Register—and initiate a reset vector fetch at address FFFC and FFFD to begin user program execution. All of the I/O ports will be initialized to the high (logic 1) state. All bits of the Control Register will be cleared causing the Interval Timer counter mode to be selected and causing all interrupt enabled bits to be reset.

7.3 RESET ($\overline{RES}$) CONDITIONS

When $\overline{RES}$ is driven from low to high the device is put in a reset state causing the registers and I/O ports to be set as shown in Table 7-1.

Table 7-1. $\overline{RES}$ Initialization of I/O Ports and Registers

BIT NO. ⟶	7	6	5	4	3	2	1	0
REGISTERS								
Processor Status	—	—	—	—	—	1	—	—
Mode Control (MCR)	0	0	0	0	0	0	0	0
Int. Enable (IER)	0	0	0	0	0	0	0	0
Int. Flag (IFR)	0	0	0	1	0	0	0	0
Host Status Flag	0	0	0	0	0	0	0	0
Input Data	0	0	0	0	0	0	0	0
Output Data	0	0	0	0	0	0	0	0
PORTS								
PA Latch	1	1	1	1	1	1	1	1
PB Latch	1	1	1	1	1	1	1	1
PC Latch	1	1	1	1	1	1	1	1
PE Latch (R6500/42 only)	1	1	1	1	1	1	1	1
PF Latch (R6500/42 only)	1	1	1	1	1	1	1	1
PG Latch (R6500/42 only)	1	1	1	1	1	1	1	1

All RAM and other CPU registers will initialize in a random, non-repeatable data pattern.

7.4 INITIALIZATION

Any initialization process for the device should include a $\overline{RES}$ as indicated in the preceding paragraphs. After stabilization of the external clock (if a power on situation) an initialization routine should be executed to perform (as a minimum) the following functions:

1. The Stack Pointer should be set
2. Clear or Set Decimal Mode
3. Set or Clear Carry Flag
4. Set up Mode Controls and Counter as required
5. Clear Interrupts.

A typical initialization routine could be as follows:

```
LDX     Load stack pointer starting address into
        X Register
TXS     Transfer X Register value to Stack Pointer
CLD     Clear Decimal Mode
SEC     Set Carry Flag
. . . .  Set-up Mode Control,
. . . .  Counter, special function
. . . .  registers and Clear RAM as required
CLI     Clear Interrupts
```

APPENDIX A
EXPANDED R6502 INSTRUCTION SET

This appendix contains a summary of the R6502 instruction set. For detailed information, consult the R6502 Microcomputer System Programming Manual, Document 29650 N30.

The four instructions notated with a * are added instructions for the IPC devices which enhance the standard 6502 instruction set.

A.1 INSTRUCTION SET IN ALPHABETIC SEQUENCE

MNEMONIC	INSTRUCTION	MNEMONIC	INSTRUCTION
ADC	Add Memory to Accumulator with Carry	LDA	Load Accumulator with Memory
AND	"AND" Memory with Accumulator	LDX	Load Index X with Memory
ASL	Shift Left One Bit (Memory or Accumulator)	LDY	Load Index Y with Memory
		LSR	Shift One Bit Right (Memory or Accumulator)
*BBR	Branch on Bit Reset Relative		
*BBS	Branch on Bit Set Relative		
BCC	Branch on Carry Clear	NOP	No Operation
BCS	Branch on Carry Set		
BEQ	Branch on Result Zero		
BIT	Test Bits in Memory with Accumulator	ORA	"OR" Memory with Accumulator
BMI	Branch on Result Minus		
BNE	Branch on Result not Zero		
BPL	Branch on Result Plus	PHA	Push Accumulator on Stack
BRK	Force Break	PHP	Push Processor Status on Stack
BVC	Branch on Overflow Clear	PLA	Pull Accumulator from Stack
BVS	Branch on Overflow Set	PLP	Pull Processor Status from Stack
		*RMB	Reset Memory Bit
CLC	Clear Carry Flag	ROL	Rotate One Bit Left (Memory or Accumulator)
CLD	Clear Decimal Mode	ROR	Rotate One Bit Right (Memory or Accumulator)
CLI	Clear Interrupt Disable Bit	RTI	Return from Interrupt
CLV	Clear Overflow Flag	RTS	Return from Subroutine
CMP	Compare Memory and Accumulator		
CPX	Compare Memory and Index X	SBC	Subtract Memory from Accumulator with Borrow
CPY	Compare Memory and Index Y	SEC	Set Carry Flag
		SED	Set Decimal Mode
DEC	Decrement Memory by One	SEI	Set Interrupt Disable Status
DEX	Decrement Index X by One	*SMB	Set Memory Bit
DEY	Decrement Index Y by One	STA	Store Accumulator in Memory
		STX	Store Index X in Memory
EOR	"Exclusive-Or" Memory with Accumulator	STY	Store Index Y in Memory
INC	Increment Memory by One		
INX	Increment Index X by One		
INY	Increment Index Y by One	TAX	Transfer Accumulator to Index X
		TAY	Transfer Accumulator to Index Y
		TSX	Transfer Stack Pointer to Index X
JMP	Jump to New Location	TXA	Transfer Index X to Accumulator
JSR	Jump to New Location Saving Return Address	TXS	Transfer Index X to Stack Register
		TYA	Transfer Index Y to Accumulator

A.2 R6500/41 AND R6500/42 INSTRUCTION SET SUMMARY TABLE

MNEMONIC	OPERATION	ADDRESSING MODE																																															PROCESSOR STATUS CODES							
		IMMEDIATE			ABSOLUTE			ZERO PAGE			ACCUM.			IMPLIED			(IND, X)			(IND), Y			Z. PAGE, X			ABS, X			ABS, Y			RELATIVE			INDIRECT			Z. PAGE, Y			BIT ADDRESSING (OP BY BIT #)								7	6	5	4	3	2	1	0
		OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	OP	n	#	0	1	2	3	4	5	6	7	N	V	·	B	D	I	Z	C
ADC	A + M + C→A (4)(1)	69	2	2	6D	4	3	65	3	2							61	6	2	71	5	2	75	4	2	7D	4	3	79	4	3																		N	V	·	·	·	·	Z	C
AND	A M→A (1)	29	2	2	2D	4	3	25	3	2							21	6	2	31	5	2	35	4	2	3D	4	3	39	4	3																		N	·	·	·	·	·	Z	·
ASL	C ← [7 Ø] ← Ø				ØE	6	3	Ø6	5	2	ØA	2	1										16	6	2	1E	7	3																					N	·	·	·	·	·	Z	C
BBR[#(Ø-7)]	Branch on M_b = Ø (5)																																								0F	1F	2F	3F	4F	5F	6F	7F	·	·	·	·	·	·	·	·
BBS[#(Ø-7)]	Branch on M_b = 1 (5)																																								8F	9F	AF	BF	CF	DF	EF	FF	·	·	·	·	·	·	·	·
BCC	Branch on C = Ø (2)																															90	2	2															·	·	·	·	·	·	·	·
BCS	Branch on C = 1 (2)																															B0	2	2															·	·	·	·	·	·	·	·
BEQ	Branch on Z = 1 (2)																															F0	2	2															·	·	·	·	·	·	·	·
BIT	A M				2C	4	3	24	3	2																																							M_7	M_6	·	·	·	·	Z	·
BMI	Branch on N = 1 (2)																															30	2	2															·	·	·	·	·	·	·	·
BNE	Branch on Z = Ø (2)																															D0	2	2															·	·	·	·	·	·	·	·
BPL	Branch on N = Ø (2)																															10	2	2															·	·	·	·	·	·	·	·
BRK	Break													00	7	1																																	·	·	·	1	·	1	·	·
BVC	Branch on V = Ø (2)																															50	2	2															·	·	·	·	·	·	·	·
BVS	Branch on V = 1 (2)																															70	2	2															·	·	·	·	·	·	·	·
CLC	Ø→C													18	2	1																																	·	·	·	·	·	·	·	0
CLD	Ø→D													D8	2	1																																	·	·	·	·	0	·	·	·
CLI	Ø→I													58	2	1																																	·	·	·	·	·	0	·	·
CLV	Ø→V													B8	2	1																																	·	0	·	·	·	·	·	·
CMP	A M	C9	2	2	CD	4	3	C5	3	2							C1	6	2	D1	5	2	D5	4	2	DD	4	3	D9	4	3																		N	·	·	·	·	·	Z	C
CPX	X M	EØ	2	2	EC	4	3	E4	3	2																																							N	·	·	·	·	·	Z	C
CPY	Y M	CØ	2	2	CC	4	3	C4	3	2																																							N	·	·	·	·	·	Z	C
DEC	M − 1→M				CE	6	3	C6	5	2													D6	6	2	DE	7	3																					N	·	·	·	·	·	Z	·
DEX	X − 1→X													CA	2	1																																	N	·	·	·	·	·	Z	·
DEY	Y − 1→Y													88	2	1																																	N	·	·	·	·	·	Z	·
EOR	AVM→A (1)	49	2	2	4D	4	3	45	3	2							41	6	2	51	5	2	55	4	2	5D	4	3	59	4	3																		N	·	·	·	·	·	Z	·
INC	M + 1→M				EE	6	3	E6															F6	6	2	FE	7	3																					N	·	·	·	·	·	Z	·
INX	X + 1→X													E8	2	1																																	N	·	·	·	·	·	Z	·
INY	Y + 1→Y													C8	2	1																																	N	·	·	·	·	·	Z	·
JMP	Jump to New Loc				4C	3	3																												6C	5	3												·	·	·	·	·	·	·	·
JSR	Jump Sub				2Ø	6	3																																										·	·	·	·	·	·	·	·
LDA	M→A (1)	A9	2	2	AD	4	3	A5	3	2							A1	6	2	B1	5	2	B5	4	2	BD	4	3	B9	4	3																		N	·	·	·	·	·	Z	·
LDX	M→X (1)	A2	2	2	AE	4	3	A6	3	2																			BE	4	3							B6	4	2									N	·	·	·	·	·	Z	·
LDY	M→Y (1)	AØ	2	2	AC	4	3	A4	3	2													B4	4	2	BC	4	3																					N	·	·	·	·	·	Z	·
LSR	Ø → [7 Ø] → C				4E	6	3	46	5	2	4A	2	1										56	6	2	5E	7	3																					Ø	·	·	·	·	·	Z	C
NOP	No Operation													EA	2	1																																	·	·	·	·	·	·	·	·
ORA	AVM→A	Ø9	2	2	ØD	4	3	Ø5	3	2							Ø1	6	2	11	5	2	15	4	2	1D	4	3	19	4	3																		N	·	·	·	·	·	Z	·
PHA	A→Ms S − 1→S													48	3	1																																	·	·	·	·	·	·	·	·
PHP	P→Ms S − 1→S													08	3	1																																	·	·	·	·	·	·	·	·
PLA	S + 1→S Ms→A													68	4	1																																	N	·	·	·	·	·	Z	·
PLP	S + 1→S Ms→P													28	4	1																																	(Restored)							
RMB[#(Ø-7)]	Ø→M_b (5)																																								Ø7	17	27	37	47	57	67	77	·	·	·	·	·	·	·	·
RØL	←[7 Ø]←[C]←				2E	6	3	26	5	2	2A	2	1										36	6	2	3E	7	3																					N	·	·	·	·	·	Z	C
RØR	→[C]→[7 Ø]→				6E	6	3	66	5	2	6A	2	1										76	6	2	7E	7	3																					N	·	·	·	·	·	Z	C
RTI	Rtrn Int													4Ø	6	1																																	(Restored)							
RTS	Rtrn Sub													6Ø	6	1																																	·	·	·	·	·	·	·	·
SBC	A − M − C→A (1)	E9	2	2	ED	4	3	E5	3	2							E1	6	2	F1	5	2	F5	4	2	FD	4	3	F9	4	3																		N	V	·	·	·	·	Z	(3)
SEC	1→C													38	2	1																																	·	·	·	·	·	·	·	1
SED	1→D													F8	2	1																																	·	·	·	·	1	·	·	·
SEI	1→I													78	2	1																																	·	·	·	·	·	1	·	·
SMB[#(Ø-7)]	1→M_b (5)																																								87	97	A7	B7	C7	D7	E7	F7	·	·	·	·	·	·	·	·
STA	A→M				8D	4	3	85	3	2							81	6	2	91	6	2	95	4	2	9D	5	3	[illegible]	5	3																		·	·	·	·	·	·	·	·
STX	X→M				8E	4	3	86	3	2																												96	4	2									·	·	·	·	·	·	·	·
STY	Y→M				8C	4	3	84	3	2													94	4	2																								·	·	·	·	·	·	·	·
TAX	A→X													AA	2	1																																	N	·	·	·	·	·	Z	·
TAY	A→Y													A8	2	1																																	N	·	·	·	·	·	Z	·
TSX	S→X													BA	2	1																																	N	·	·	·	·	·	Z	·
TXA	X→A													8A	2	1																																	N	·	·	·	·	·	Z	·
TXS	X→S													9A	2	1																																	·	·	·	·	·	·	·	·
TYA	Y→A													98	2	1																																	N	·	·	·	·	·	Z	·

NOTES

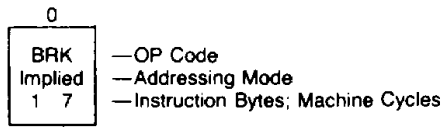
1. Add 1 to N if page boundary is crossed
2. Add 1 to N if branch occurs to same page
   Add 2 to N if branch occurs to different page
3. Carry not = Borrow
4. If in decimal mode Z flag is invalid
   accumulator must be checked on zero result.
5. Effects 8-bit data field of the specified zero page address.

LEGEND

- X = Index X
- Y = Index Y
- A = Accumulator
- M = Memory per effective address
- M_s = Memory per stack pointer
- M_b = Selecter zero page memory bit
- M_7 = Memory Bit 7
- M_6 = Memory Bit 6
- + = Add
- − = Subtract
- ∧ = And
- V = Or
- ⊻ = Exclusive Or
- n = Number of cycles
- # = Number of Bytes

3

A.3 INSTRUCTION CODE MATRIX

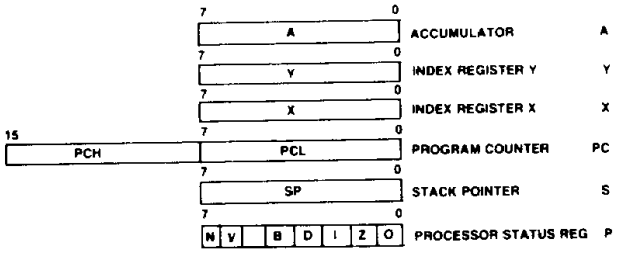


MSD \ LSD	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	
0	BRK Implied 1 7	ORA (IND, X) 2 6				ORA ZP 2 3	ASL ZP 2 5	RMB0 ZP 2 5	PHP Implied 1 3	ORA IMM 2 2	ASL Accum 1 2			ORA ABS 3 4	ASL ABS 3 6	BBR0 ZP 3 5**	0
1	BPL Relative 2 2**	ORA (IND), Y 2 5*				ORA ZP, X 2 4	ASL ZP, X 2 6	RMB1 ZP 2 5	CLC Implied 1 2	ORA ABS, Y 3 4*				ORA ABS, X 3 4*	ASL ABS, X 3 7	BBR1 ZP 3 5**	1
2	JSR Absolute 3 6	AND (IND, X) 2 6			BIT ZP 2 3	AND ZP 2 3	ROL ZP 2 5	RMB2 ZP 2 5	PLP Implied 1 4	AND IMM 2 2	ROL Accum 1 2		BIT ABS 3 4	AND ABS 3 4	ROL ABS 3 6	BBR2 ZP 3 5**	2
3	BMI Relative 2 2**	AND (IND, Y) 2 5*				AND ZP, X 2 4	ROL ZP, X 2 6	RMB3 ZP 2 5	SEC Implied 1 2	AND ABS, Y 3 4*				AND ABS, X 3 4*	ROL ABS, X 3 7	BBR3 ZP 3 5**	3
4	RTI Implied 1 6	EOR (IND, X) 2 6				EOR ZP 2 3	LSR ZP 2 5	RMB4 ZP 2 5	PHA Implied 1 3	EOR IMM 2 2	LSR Accum 1 2		JMP ABS 3 3	EOR ABS 3 4	LSR ABS 3 6	BBR4 ZP 3 5**	4
5	BVC Relative 2 2**	EOR (IND), Y 2 5*				EOR ZP, X 2 4	LSR ZP, X 2 6	RMB5 ZP 2 5	CLI Implied 1 2	EOR ABS, Y 3 4*				EOR ABS, X 3 4*	LSR ABS, X 3 7	BBR5 ZP 3 5**	5
6	RTS Implied 1 6	ADC (IND, X) 2 6				ADC ZP 2 3	ROR ZP 2 5	RMB6 ZP 2 5	PLA Implied 1 4	ADC IMM 2 2	ROR Accum 1 2		JMP Indirect 3 5	ADC ABS 3 4	ROR ABS 3 6	BBR6 ZP 3 5**	6
7	BVS Relative 2 2**	ADC (IND, Y) 2 5*				ADC ZP, X 2 4	ROR ZP, X 2 6	RMB7 ZP 2 5	SEI Implied 1 2	ADC ABS, Y 3 4*				ADC ABS, X 3 4*	ROR ABS, X 3 7	BBR7 ZP 3 5**	7
8		STA (IND, X) 2 6			STY ZP 2 3	STA ZP 2 3	STX ZP 2 3	SMB0 ZP 2 5	DEY Implied 1 2		TXA Implied 1 2		STY ABS 3 4	STA ABS 3 4	STX ABS 3 4	BBS0 ZP 3 5**	8
9	BCC Relative 2 2**	STA (IND, Y) 2 6			STY ZP, X 2 4	STA ZP, X 2 4	STX ZP, Y 2 4	SMB1 ZP 2 5	TYA Implied 1 2	STA ABS, Y 3 5	TXS Implied 1 2			STA ABS, X 3 5		BBS1 ZP 3 5**	9
A	LDY IMM 2 2	LDA (IND, X) 2 6	LDX IMM 2 2		LDY ZP 2 3	LDA ZP 2 3	LDX ZP 2 3	SMB2 ZP 2 5	TAY Implied 1 2	LDA IMM 2 2	TAX Implied 1 2		LDY ABS 3 4	LDA ABS 3 4	LDX ABS 3 4	BBS2 ZP 3 5**	A
B	BCS Relative 2 2**	LDA (IND), Y 2 5*			LDY ZP, X 2 4	LDA ZP, X 2 4	LDX ZP, Y 2 4	SMB3 ZP 2 5	CLV Implied 1 2	LDA ABS, Y 3 4*	TSX Implied 1 2		LDY ABS, X 3 4*	LDA ABS, X 3 4*	LDX ABS, Y 3 4*	BBS3 ZP 3 5**	B
C	CPY IMM 2 2	CMP (IND, X) 2 6			CPY ZP 2 3	CMP ZP 2 3	DEC ZP 2 5	SMB4 ZP 2 5	INY Implied 1 2	CMP IMM 2 2	DEX Implied 1 2		CPY ABS 3 4	CMP ABS 3 4	DEC ABS 3 6	BBS4 ZP 3 5**	C
D	BNE Relative 2 2**	CMP (IND), Y 2 5*				CMP ZP, X 2 4	DEC ZP, X 2 6	SMB5 ZP 2 5	CLD Implied 1 2	CMP ABS, Y 3 4*				CMP ABS, X 3 4*	DEC ABS, X 3 7	BBS5 ZP 3 5**	D
E	CPX IMM 2 2	SBC (IND, X) 2 6			CPX ZP 2 3	SBC ZP 2 3	INC ZP 2 5	SMB6 ZP 2 5	INX Implied 1 2	SBC IMM 2 2	NOP Implied 1 2		CPX ABS 3 4	SBC ABS 3 4	INC ABS 3 6	BBS6 ZP 3 5**	E
F	BEQ Relative 2 2**	SBC (IND), Y 2 5*				SBC ZP, X 2 4	INC ZP, X 2 6	SMB7 ZP 2 5	SED Implied 1 2	SBC ABS, Y 3 4*				SBC ABS, X 3 4*	INC ABS, X 3 7	BBS7 ZP 3 5**	F
	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F	

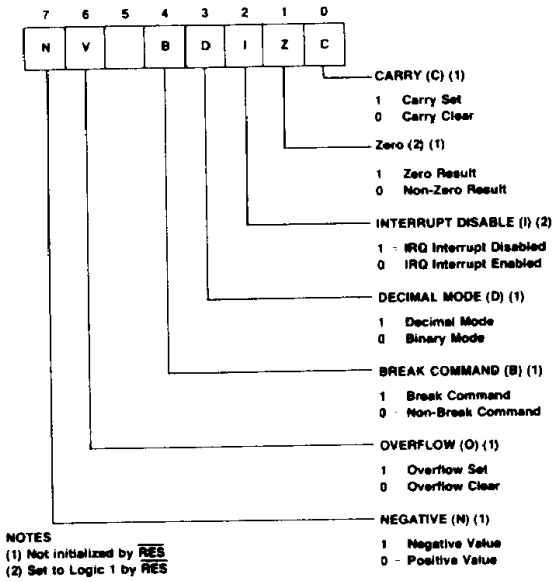
*Add 1 to N if page boundary is crossed.
**Add 1 to N if branch occurs to same page;
add 2 to N if branch occurs to different page.

APPENDIX B
KEY REGISTER SUMMARY

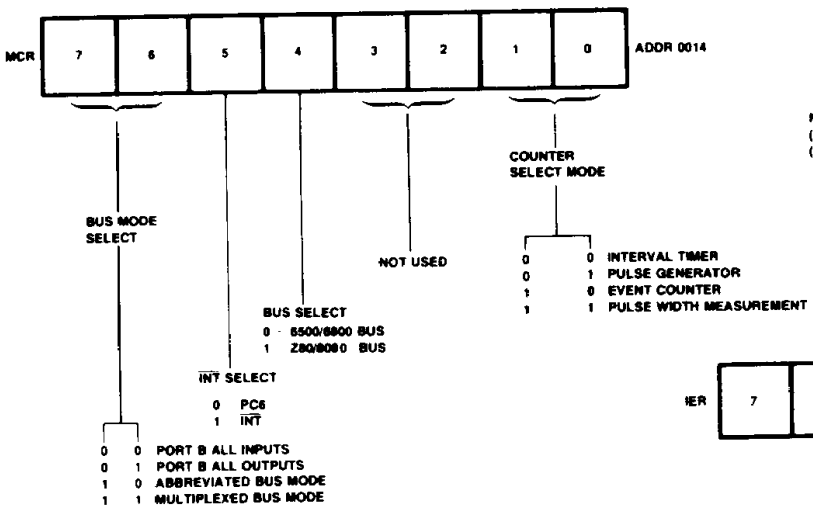
CPU Registers



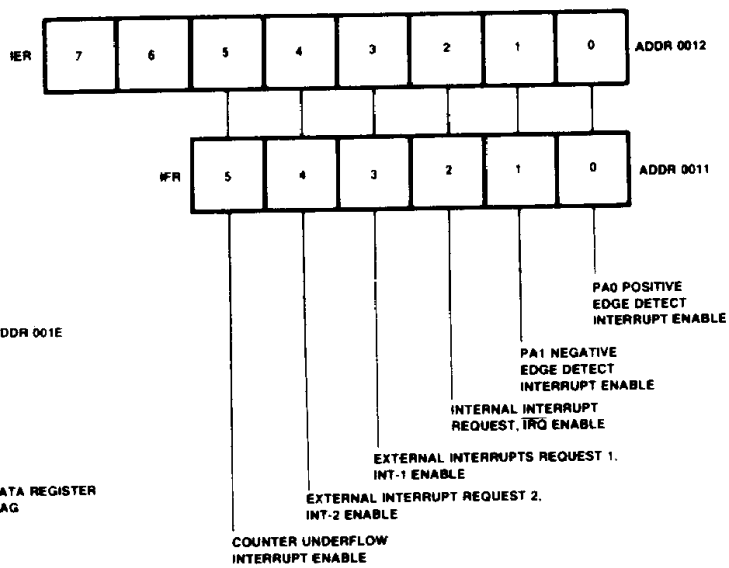
Processor Status Register



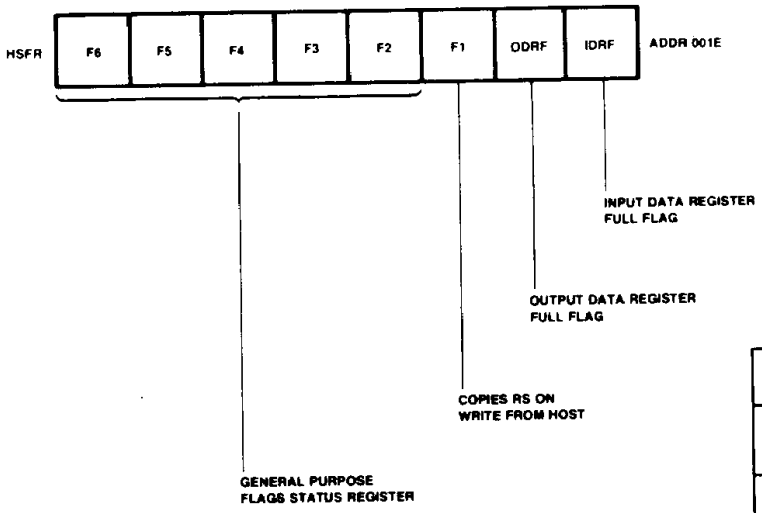
Mode Control Register



Interrupt Enable and Flag Registers



Host Status Flag Register

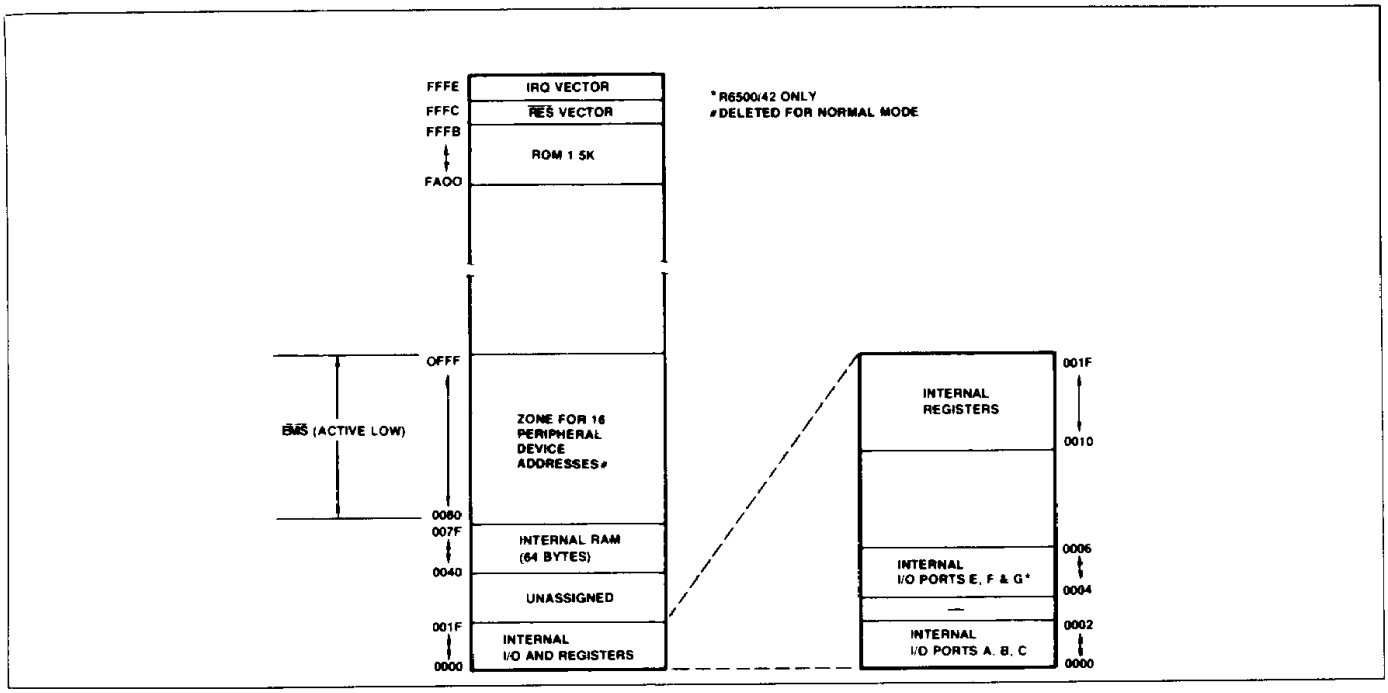


Host Addressing Matrix

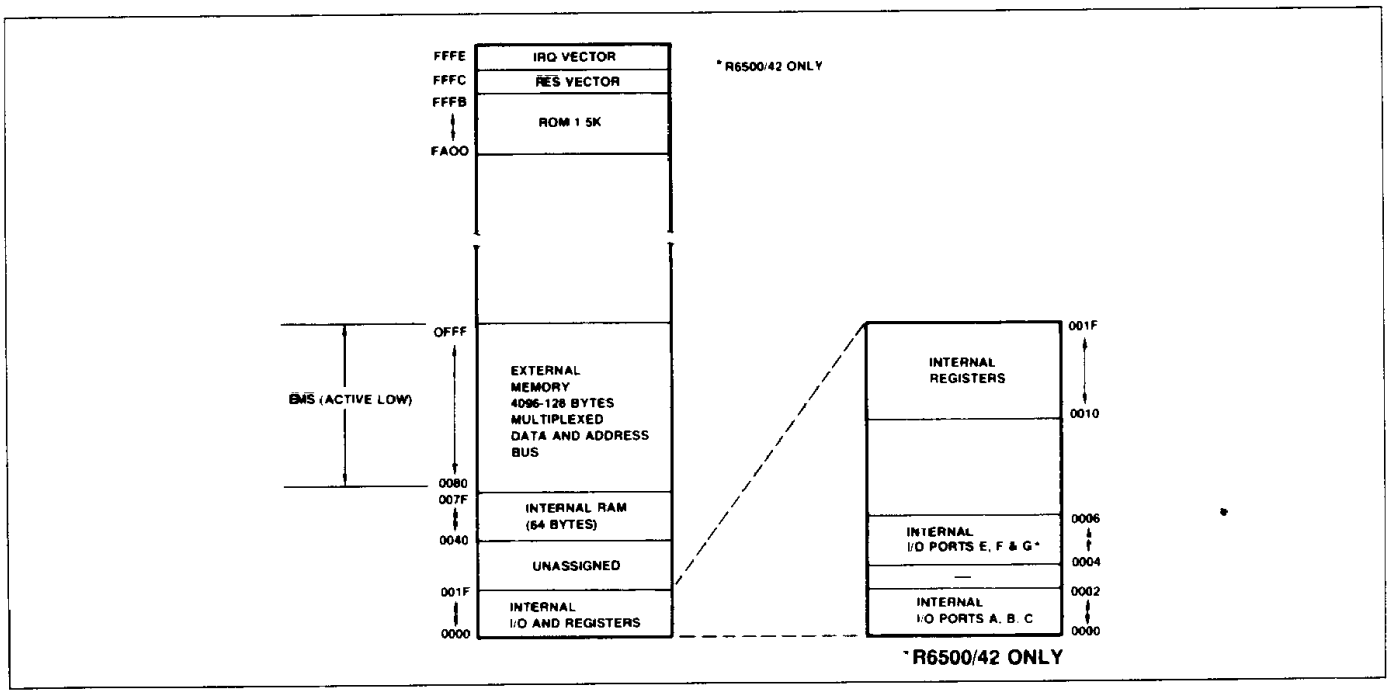
RS (A_0)	READ	WRITE
1	HOST STATUS FLAG	COMMAND INPUT
0	DATA REG OUTPUT	DATA REG INPUT

APPENDIX C
MEMORY MAPS AND ADDRESS AND PIN ASSIGNMENTS

C.1 ABBREVIATED BUS MODE MEMORY MAP



C.2 MULTIPLEXED BUS MODE MEMORY MAP



C.3 I/O AND INTERNAL REGISTER ADDRESSES

ADDRESS	READ	WRITE
001F	— —	— —
1E	Host Status Flag Register	Host Status Flag Register
1D	— —	— —
1C	Input Data Register (IDR)	Output Data Register (ODR)
1B	— —	— —
1A	Lower Counter	Lower Latch
19	Lower Counter & Clear Flag (IFR5)	Upper Latch/Transfer Latch to Counter & Clear Flag (IFR5)
18	Upper Counter	Upper Latch
17	— —	— —
16	— —	— —
15	— —	— —
14	Mode Control Register	Mode Control Register
13	— —	— —
12	Interrupt Enable Register	Interrupt Enable Register
11	Interrupt Flag Register	— —
10	Read "FF"	Clear Int Flag Bit
0F	— —	— —
0E	— —	— —
0D	— —	— —
0C	— —	— —
0B	— —	— —
0A	— —	— —
09	— —	— —
08	— —	— —
07	— —	— —
06	Port G (R6500/42 only)	Port G (R6500/42 only)
05	Port F (R6500/42 only)	Port F (R6500/42 only)
04	Port E (R6500/42 only)	Port E (R6500/42 only)
03	— —	— —
02	Port C	Port C
01	Port B	Port B
00	Port A	Port A

C.4 MULTIPLE FUNCTION PIN ASSIGNMENTS

PIN NUMBER R6500/41	PIN NUMBER R6500/42	I/O FUNCTION	ABBREVIATED PORT FUNCTION	MULTIPLEXED PORT FUNCTION
13	16	PC0	A0	A0
14	17	PC1	A1	A1
15	18	PC2	A2	A2
16	19	PC3	A3	A3
17	20	PC4	R/$\overline{W}$	R/$\overline{W}$
18	21	PC5	$\overline{EMS}$	$\overline{EMS}$
19	22	PC6/$\overline{INT}$	PC6/$\overline{INT}$	PC6/$\overline{INT}$
30	49	PB0	D0	A4/D0
31	50	PB1	D1	A5/D1
32	51	PB2	D2	A6/D2
33	52	PB3	D3	A7/D3
34	53	PB4	D4	A8/D4
35	54	PB5	D5	A9/D5
36	55	PB6	D6	A10/D6
37	56	PB7	D7	A11/D7

MAXIMUM RATINGS*

Parameter	Symbol	Value	Unit
Supply Voltage	V_{CC}	−0.3 to +7.0	Vdc
Input Voltage	V_{IN}	−0.3 to +7.0	Vdc
Operating Temperature Commercial	T_A	T_L to T_H 0 to +70	°C
Storage Temperature	T_{STG}	−55 to +150	°C

***NOTE:** Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the other sections of this document is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

DC CHARACTERISTICS

(V_{CC} = 5.0V ±5%, V_{SS} = 0V; T_A = 0° to 70°C, unless otherwise specified)

Parameter	Symbol	Min	Typ[1]	Max	Unit	Test Conditions
Input High Voltage	V_{IH}	+2.0	—	V_{CC}	V	
Input Low Voltage	V_{IL}	−0.3	—	+0.8	V	
Input Leakage Current $\overline{RES}$, $\overline{NMI}$	I_{IN}	—	—	±10.0	μA	V_{IN} = 0 to 5.0V
Input Low Current	I_{IL}	—	−1.0	−1.6	mA	V_{IL} = 0.4V
Output High Voltage	V_{OH}	+2.4	—	V_{CC}	V	I_{LOAD} = −100 μA V_{CC} = 4.75V
Output High Voltage (CMOS)	V_{CMOS}	V_{CC}−30%	—	V_{CC}	V	V_{CC} = 4.75V
Output Low Voltage	V_{OL}	—	—	+0.4	V	I_{LOAD} = 1.6 mA V_{CC} = 4.75V
I/O Port Pull-Up Resistance PA0–PA7, PC0–PC7, PF0–PF7[3], PG0–PG7[3]	R_L	3.0	6.0	11.5	Kohm	
Output High Current (Sourcing)	I_{OH}	−100	—	—	μA	V_{OH} = 2.4V
Output Low Current (Sinking, PE[3])	I_{OL}	1.6	—	—	mA	V_{OL} = 0.4V
Darlington Current Drive (PE[3])	I_{OH}	−1.0	—	—	mA	V_{OH} = 1.5V
Input Capacitance PA, PB, PC, PF[3], PG[3]	C_{IN}	—	—	10	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Output Capacitance (Three-State Off)	C_{OUT}	—	—	10	pF	T_A = 25°C V_{IN} = 0V f = 1.0 MHz
Power Dissipation (Outputs High)	P_D	—	550	1050	mW	T_A = 25°C

Notes:
1. Typical values measured at T_A = 25°C and V_{CC} = 5.0V.
2. Negative sign indicates outward current flow, positive indicates inward flow.
3. R6500/42 only.

APPENDIX E
TIMING REQUIREMENTS AND CHARACTERISTICS

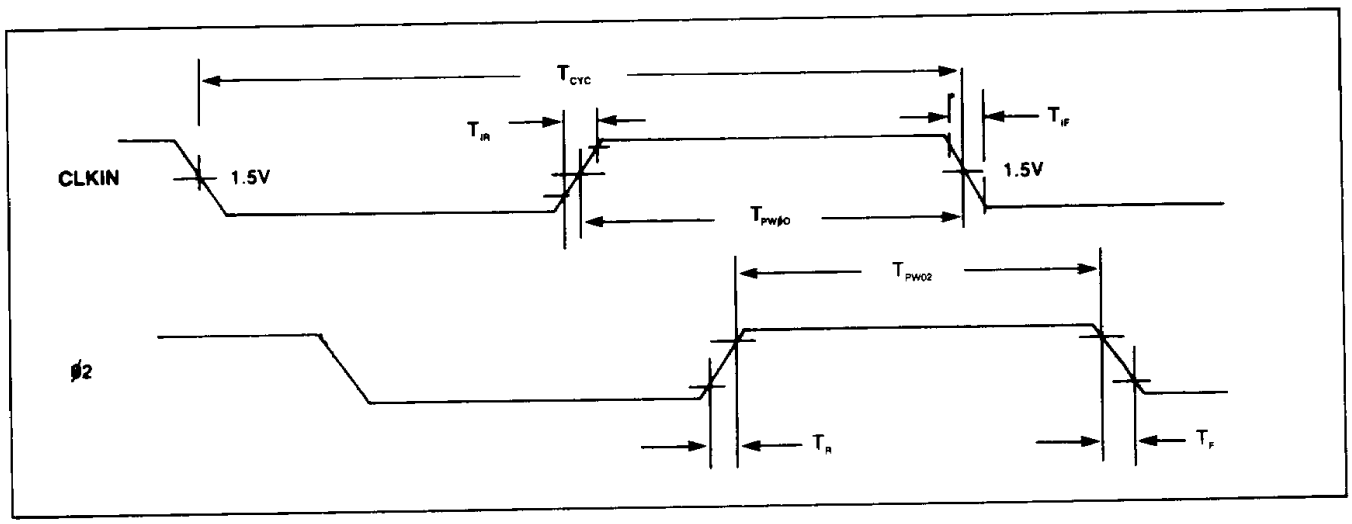
E.1 GENERAL NOTES

1. V_{CC} 5V ± 5%, 0 C ≤ TA ≤ 70 C
2. A valid V_{CC} — RES sequence is required before proper operation is achieved.
3. All timing reference levels are 0.8V and 2.0V, unless otherwise specified.
4. All time units are nanoseconds, unless otherwise specified.
5. All capacitive loading is 130pf maximum, except as noted below:

PA, PB	—	50pf maximum
PB, PC (I/O Modes Only)	—	50pf maximum
PB, PC (ABB and Mux Mode)	—	130pf maximum

E.2 CLOCK TIMING

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{CYC}	Cycle Time	1000	10 μs	500	10 μs
$T_{PW\phi O}$	CLKIN Input Clock Pulse Width	475	—	240	—
T_{PW02}	Output Clock Pulse Width at Minimum T_{CYC}	$T_{PW\phi O}$	$T_{PW\phi O}$ +25	$T_{PW\phi O}$	$T_{PW\phi O}$ +20
T_R, T_F	Output Clock Rise, Fall Time	—	25	—	15
T_{IR}, T_{IF}	Input Clock Rise, Fall Time	—	10	—	10



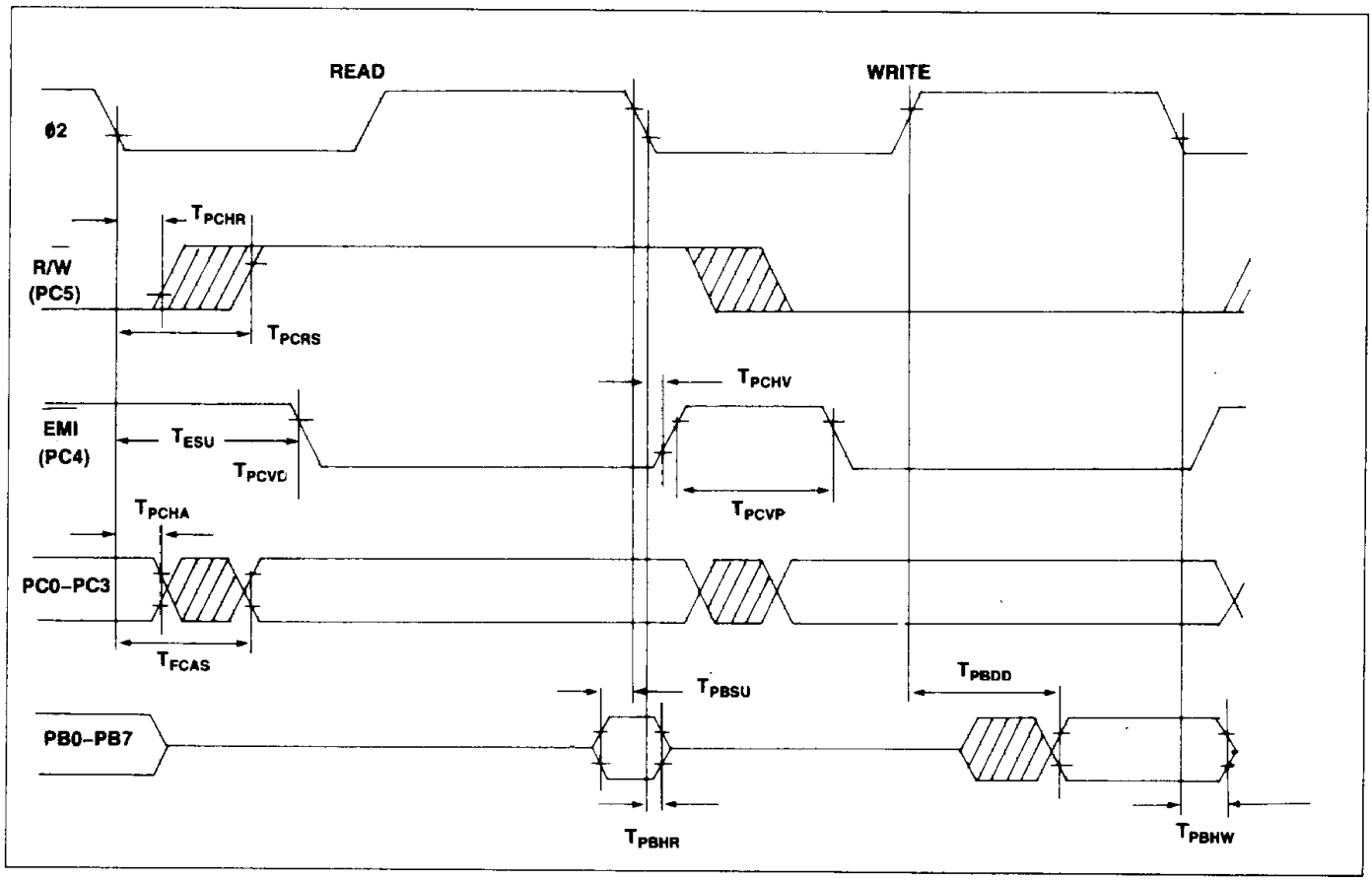
E.3 ABBREVIATED MODE TIMING—PB AND PC

(MCR 5 = 1, MCR 6 = 0, MCR 7 = 1)

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{PCRS}	(PC5) R/W Setup Time	—	225	—	140
T_{PCAS}	(PC0-PC3) Address Setup Time	—	225	—	140
T_{PBSU}	(PB) Data Setup Time	50	—	35	—
T_{PBHR}	(PB) Data Read Hold Time	10	—	10	—
T_{PBHW}	(PB) Data Write Hold Time	30	—	30	—
T_{PBDD}	(PB) Data Output Delay	—	175	—	150
T_{PCHA}	(PC0-PC3) Address Hold Time	30	—	30	—
T_{PCHR}	(PC5) R/W Hold Time	30	—	30	—
T_{PCHV}	(PC4) $\overline{EMS}$ Hold Time	10	—	10	—
T_{PCVP}	(PC4) $\overline{EMS}$ Stabilization Time	30	—	30	—
T_{ESV}	$\overline{EMS}$ Setup Time	—	350	—	210

NOTE 1: Values assume PC0-PC5 have the same capacitive load.

E.3.1 Abbreviated Mode Timing Diagram



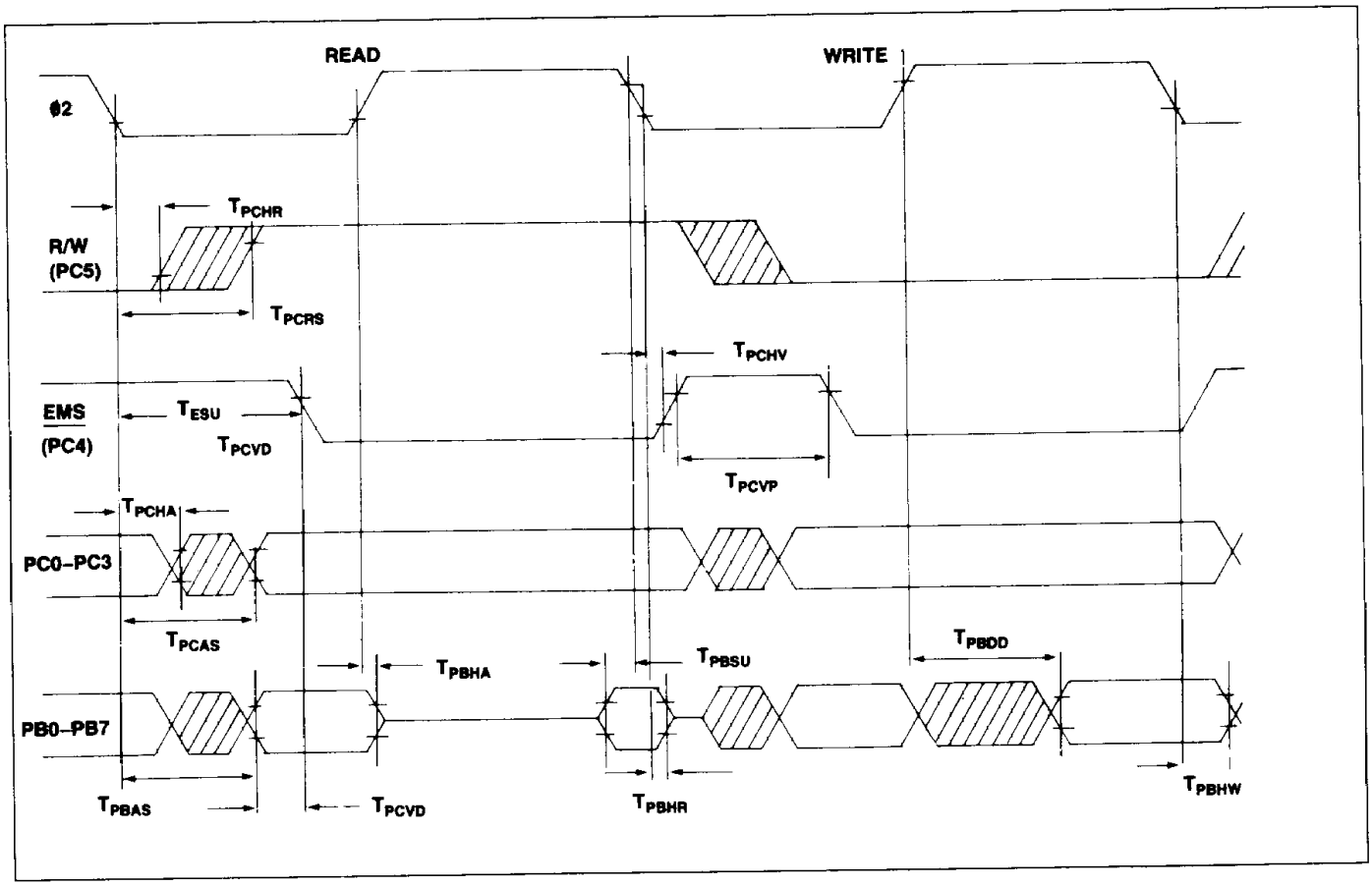
E.4 MULTIPLEXED MODE TIMING—PB AND PC

(MCR 5 = 1, MCR 6 = 1, MCR 7 = 1)

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
T_{PCRS}	(PC5) R/W Setup Time	—	225	—	140
T_{PCAS}	(PC0-PC3) Address Setup Time	—	225	—	140
T_{PBAS}	(PB) Address Setup Time	—	225	—	140
T_{PBSU}	(PB) Data Setup Time	50	—	35	—
T_{PBHR}	(PB) Data Read Hold Time	10	—	10	—
T_{PBHW}	(PB) Data Write Hold Time	30	—	30	—
T_{PBDD}	(PB) Data Output Delay	—	175	—	150
T_{PCHA}	(PC0-PC3) Address Hold Time	30	—	30	—
T_{PBHA}	(PB) Address Hold Time	0	100	0	80
T_{PCHR}	(PC5) R/W Hold Time	30	—	30	—
T_{PCHV}	(PC4) $\overline{EMS}$ Hold Time	10	—	10	—
T_{PCVD}(1)	(PC4) Address to $\overline{EMS}$ Delay Time	30	—	30	—
T_{PCVP}	(PC4) $\overline{EMS}$ Stabilization Time	30	—	30	—
T_{ESU}	$\overline{EMS}$ Setup Time	—	350	—	210

NOTE 1: Values assume PC0-PC5 have the same capacitive load.

E.4.1 Multiplex Mode Timing Diagram



E.5 I/O, EDGE DETECT AND COUNTER TIMING

SYMBOL	PARAMETER	1 MHz		2 MHz	
		MIN	MAX	MIN	MAX
	Internal Write to Peripheral Data Valid				
T_{PDW}[1]	PA, PC TTL	—	500	—	500
T_{CMOS}[1]	PA, PC CMOS	—	1000	—	1000
T_{PDDW}	PB	—	175	—	150
	Peripheral Data Setup Time				
T_{PDSU}	PA, PC	200	—	200	—
T_{PDSU}	PB	50	—	50	—
	Peripheral Data Hold Time				
T_{PHR}	PA, PC	75	—	75	—
T_{PHR}	PB	10	—	10	—
T_{EPW}	PA0-PA1 Edge Detect Pulse Width	T_{CYC}	—	T_{CYC}	—
	Counter				
T_{CPW}	PA2 Input Pulse Width	T_{CYC}	—	T_{CYC}	—
T_{CD}[1]	PA2 Output Delay	—	500	—	500

NOTE 1: Maximum Load Capacitance: 50pF Passive Pull-Up Required

E.5.1 I/O, Edge Detect, Counter